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Analysis of Booth Multiplier based Conventional and Short Word Length FIR Filter

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ABSTRACT

The optimized implantation of digital filters has remained one of the challenging tasks, for FPGA (Field-Programmable Gate Array) based system designers, due to the involvement of very complex circuitry for multiplication. The multiplier consumes more recourse and hence results in less speed, being not the single step arithmetic operation. One way to carry out these implementations effectively is; to reduce the word length that will increase throughput in view of that. Since decays, SDM (Sigma-Delta Modulation) isused to convert the word length from multi-bit to single bit recurrently. This work is an extension of current trends of using SDM, in the design of Digital FIR (Finite Impulse Response) Filter, which is the most attractive component of DSP (Digital Signal Processor)

In this work, we have presented single-bit ternary (0,+1,-1) and multi-bit FIR filterdesign, using the Booth multiplier technique, on small commercially used FPGA family, provided by Altera. Also, the performance analysis of designed filter with SWL (Short Word Length) using SDM and the conventional one (Multi-bit FIR Filter using general booth multiplier) is carried out.

The results indicate that with consuming the resources one third of the conventional design, the sigma delta modulation based multiplier results six times more efficient in terms of achieved frequency, hence sum up the reason of using the sigma delta modulation in about all DSP applications.

Key Words: Short Word Length, Sigma Delta Modulatio, Finite Impulse Response Filter, Altera Field Programmable Gate Arrays.

1. INTRODUCTION

When compared to multi-bit systems, the single bit systems are intrinsically much simpler, making them widely used in various digital processing systems, along with audio processing [1]. Multipliers are the most area and power consuming elements in DSP [2]. Systems that are loaded with heavy multiplication often become trivial in the single-bit domain [3].

In a few decades, the SDM technique has broaden its domain of applications, from being used in analog to digital convertor to very complex DSP system design [4]. The SSDM is a specific method to convert low-bandwidth signals into a digital data stream [5]. This is key element in developing single-bit processing algorithms [6].

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SDM has successively grappled the DSP; as this technique results in small word length at output, for comparatively large input. The small or short word length output is used as the input of another DSP system, causing those systems to process lesser data hence performing more efficiently.

A good list of publication has shown the plug in of SDM technique in so many DSP systems, implemented on FPGA, including single bit FIR filtering. The implementation of single bit FIR and IIR filter was first seen in [7,8] . The same was observed in [8]], the design of a single bit FIR technique with bit stream input and fixed or floating point coefficients is also reported in [9,10]. With comparison to [7,8] in [9] the decoder is replaced by a ΣΔM having low pass signal transfer function. While the filter coefficients in [10] are generated at the Nyquist rate.

The design approach of a SBTFF (Single-Bit Ternary FIR-Like Filter) mentioned in [11,12] is implemented on small commercial FPGAs, using Quartus-II simulator. The motive of the design is to compare its power-area-performance characteristics with approximately equivalent muti-bit FIR filters. It is shown that SBTFF is dominant over its counterpart muti-bit system except at very extreme number of coefficients (i.e. 8192/18 bits width of coefficients).

Memon and Beckett [13], have reported the impact of alternative encoding techniques namely twos complement, RBSD (Redundancy Binary Signed Digit), and CSD (Canonical Signed Digit) for SBT algorithms. It is reported that RBSD occupies double the space with poor performance compared to two's complement. Unlike multibit system, CSD has no extra advantage over twos complement in single-bit domain DSP algorithms using SDMs.

In [14], Booth and Wallace tree multiplier were compared on the basis of area-performance and results show a tradeoff between two algorithms. Simulation indicate that Booth offers better performance with more chip area than Wallace tree.

In this work, we have extended the work reported above and compared Booth algorithms area-performance for SBT-FIR-like filter and multi-bit FIR filter using two small commercial FPGA devices provided by the Altera.

This paper proceeds as follows. In section 2, SSBT-FIR filter is described. Section 3 shows Booth Multiplier algorithm and its flow diagram. FPGA based design and implementation is shown in section 4. While the results and discussions are given in section 5 and finally the work is concluded in section 6.

2. SINGLE BIT TERNARY FIR FILTER

FIR filters are digital filters with impulse response of finite duration, because it settles to zero in finite time [15]. The FIR filters (Fig. 1) are stable with linear phase. These inherent characteristics make them to be used in various signal processing applications [16].

The motive of the digital filter is to take an input sequence, and produce a different output sequences, depending on the impulse response of the filter [18].

As clearly indicated by name, FIR filters process a fine number of sample values, reducing the convolution sum to a finite sum per output sample instant [16,19].

The output of an FIR of order or length L, to an input time-series x[n], is given by a finite version of the convolution sum given in Equation (1), namely:

$$Y[n] = x[n] * f[n] = \sum_{k=0}^{n-1} f[k]x[n-k] \quad (1)$$

Where; f[0] ≠ 0 through f [L-1] ≠ 0 are the filter's L coefficients [20,21].

3. BOOTH ALGORITHM

In the multiplier considered here, two's complement binary number representations are used at the inputs and the output [22]. Booth's Algorithm (Fig. 2) is a smart move for multiplying signed number. It initiate with the ability to both add and subtract [23]. Booth multiplication algorithm consists of three major steps; generation of partial product called as recoding, reducing the partial product in two rows, and addition that gives final product [24].

(a) Flow Diagram

The steps involved in Booth algorithm is given as below:

(b) Algorithms

Step-1

(a) Decide the multiplier and then multiplicand.

(b) Initialize the remaining registers to '0'.

(c) Initialize count register with number of multiplicand bits.

(d) To determine the specific arithmetic action, use the current LSB (Least Significant Bit)

(e) and the previous LSB. For Example:

- Multiplicand =7 → 0111 → M
- Multiplier =3 → 0011 → Q
- Register 'A' =0 → 0000 → A
- Register Q-1 =0 → 0000 → Q-1
- Register Count =4 → 0100 → Count

Step-2

(a) Possible arithmetic actions:

- 00 no arithmetic operation
- 11 no arithmetic operation
- 10 add multiplicand to left half of product
- 01 subtract multiplicand from left half of product

Step-3

(a) Perform an ASR (Arithmetic Right Shift) on the entire product.

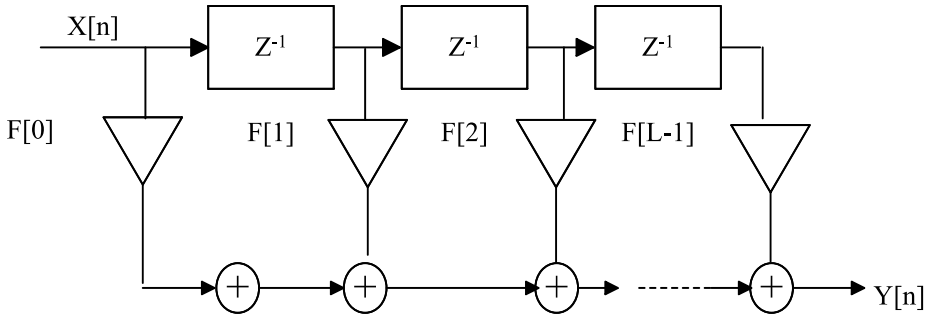

FIG. 1. FIR FILTER [17]

Step-4

(a) When count register is not '0' then continue the multiplication.

If count register is '0' then END the algorithm

4. FPGA BASED IMPLEMENTATION

The FPGA based implementation of the FIR filter (Fig. 3) is carried out in to two stages. In the first stage, the 2 bit booth multiplier is designed, to perform the task of multiplication, ofthe data and filter weight.

While the data and the required filter weights are primarily converted to single bit by using the SDM. In the second phase, by incorporating the deigned Booth Multiplier, and the two bit adder, the FIR filter is implemented.

Besides, to compare the performance of single bit design, with multi-bit implementation, the results from a previous published work given in [14] are use, where the 6, 8 and 10 bit Booth Multiplier was designed and incorporated in to 8 tab fir filter.

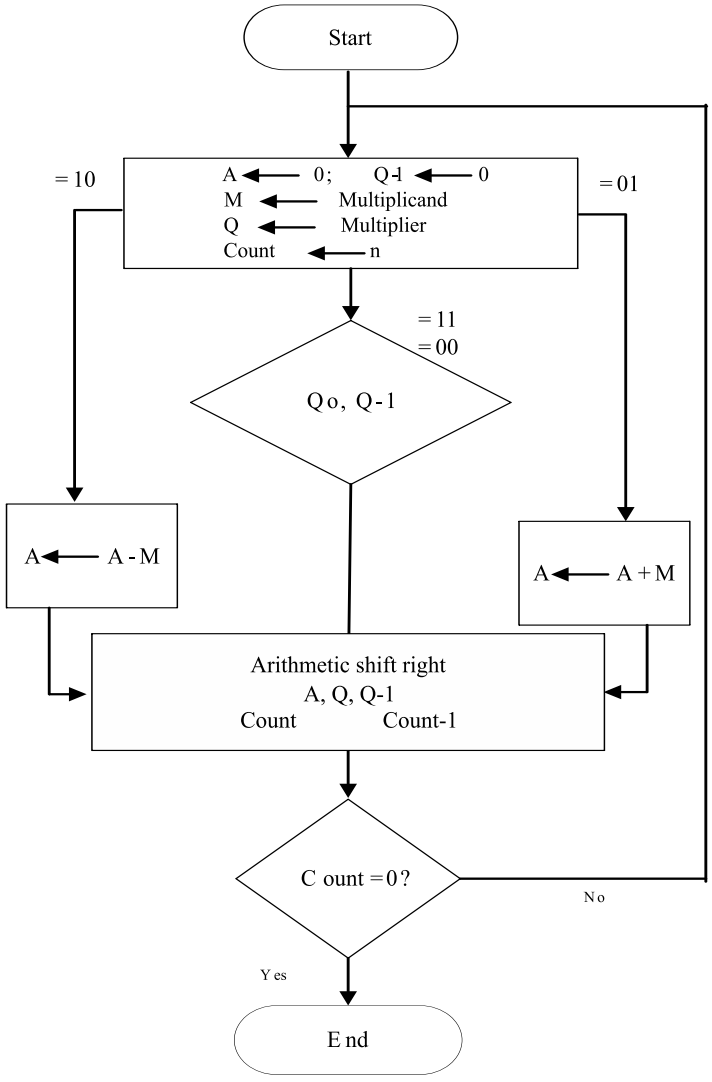

FIG. 2. BOOTH MULTIPLIER FLOW DIAGRAM

5. RESULTS AND DISCUSSION

The performance analysis of FPGA based implementation of short word length (single bit)and multi-bit booth multiplier, along with design of concerned bit FIR filter is tabulated as under.

In the design, comparison of 2, 6, 8, and 10 bit multiplier is carried out, whereas the tab of the filter is keep to 8 overall.

In this work, two commercially used, small FPGAs from the Altera family were used as the development board, and hence the implementation results show that, with the one third of the consumed logic blocks at average; in comparison to the other three implementations, the SDM based coded booth multiplier performs very well, in terms of achieved frequency.

Tables1-4 on the other hand strengthen the worth of SDM to be used in DSP systems, as it is obvious from the results that, FIR Filter, designed using single bit booth multiplier consume very less resources in conjunction with observable performance in terms of frequency; as frequency achieved is even much greater than for 6, 8 and 10 bit Multiplier based FIR Filter..

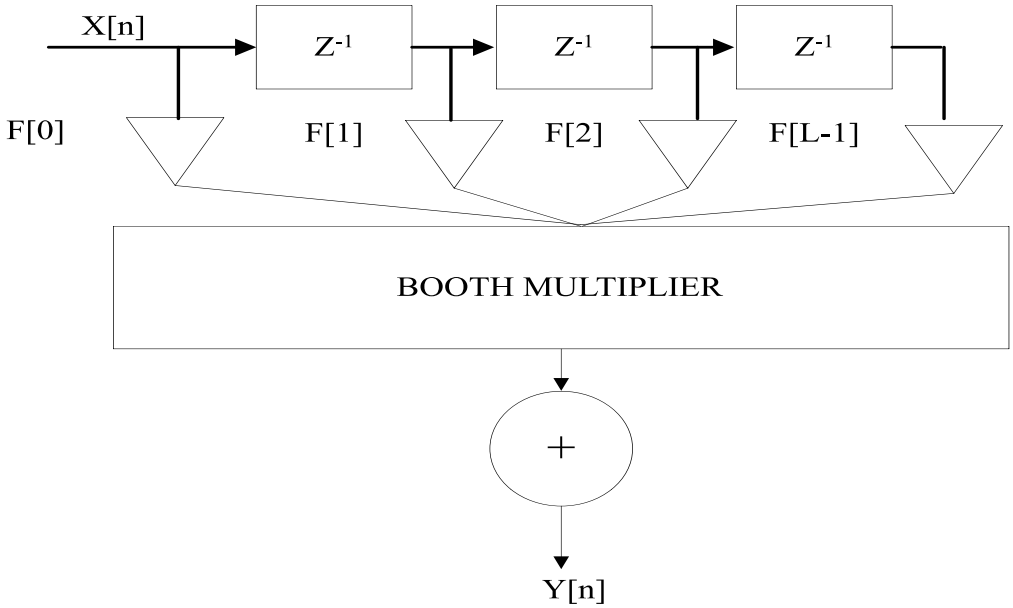

FIG. 3. FIR FILTER DESIGN BOOTH MULTIPLIER

TABLE 1. AREA PERFORMANCE OF CYCLONE FPGA BASED BOOTH MULTIPLIER

No.	FPGA	Bit Width	LUTS	Logic Reg:	F_{max}(MHz)
1.	Cycloone	2 (SDM)	43	15	196.54
2.		6	116	23	118.34
3.		8	147	27	127.23
4.		10	177	31	105.29

TABLE 3. PERFORMANCE ANALYSIS OF SINGLE BIT AND MULTIBIT FIR FILTER USING BOOTH MULTIPLIER IN CYCLONE II

No.	FPGA	Bit Width	Filter Tap	Combinational ALUTs	F^{max} (MHz)
1.	Cycloone	2 (SDM)	8	6	319.49
2.		6		3925	46.2
3.		8		14368	35.3
4.		10		28499	29.1

TABLE 4. PERFORMANCE ANALYSIS OF SINGLE BIT AND MULTIBIT FIR FILTER USING BOOTH MULTIPLIER IN STRATIX III

No.	FPGA	Bit Width	Filter Tap	Combinational ALUTs	F_{max} (MHz)
1.	Stratix	2 (SDM)	8	9	324.04
2.		6		2977	86.5
3.		8		10653	69.1
4.		10		20287	57.5

6. CONCLUSION

As the SWL based system design consume less resource, and results in considerable performance efficiency in terms of achieved frequency, this work may be concluded as; if the SWL algorithm is forced to be used in DSP systems, they will bring very fruitful result.

Hence this work indicates the importance of SWL processing achieved with a unit, known as SDM.

The continuity of this work would be carried out by author, by using the SDM in the design of very generic adaptive filters.

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REFERENCES

[1] Memon, T.D., Beckett, P., and Hussain, Z.M., "Analysis and Design of a Ternary FIR Filter Using Sigma Delta Modulation", IEEE 13th International Multitopic Conference, pp. 1-5, December, 2009.

[2] Barsainya, R., Agarwal, M., and Rawat, T.K., "Design and FPGA Implementation of Multiplierless Comb Filter", International Journal of Circuit Theory and Applications, 2017.

[3] Sadik, A.Z., Hussain, Z.M., and O'Shea, P., "A Single-Bit Digital DC-Blocker using Ternary Filtering", Proceedings of IEEE TENCON, pp. 1-6, November, 2005.

[4] Memon, T., Beckett, P., and Sadik, A.Z., "Sigma-Delta Modulation Based Digital Filter Design Techniques in FPGA", ISRN Electronics, pp. 10, 2012.

[5] Pelgrom, P., "Sigma-Delta Modulation", Analog-to-Digital Conversion", Springer International Publishing, pp. 441-506, 2017.

[6] Aziz, P.M., Sorensen, H.V., and Vn der Spiege, l.J., "An Overview of Sigma-Delta Converters", IEEE Signal Processing Magazine, Volume 13, pp. 61-84, 1996.

[7] Johns, D.A., and Lewis, D.M., "Design and Analysis of Delta-Sigma Based IIR Filters", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Volume 40, pp. 233-240, 1993.

[8] Kershaw, S.M., Summerfield, S., Sandler, M.B., and Anderson, M., "Realization and Implementation of a Sigma-Delta Bitstream FIR Filter", IEE Proceedings on Circuits, Devices and Systems, Volume 143, pp. 267-273, 1996.

[9] Wong, P.W., and Gray, R.M., "FIR Filters with Sigma-Delta Modulation Encoding", IEEE Transactions on Acoustics, Speech, and Signal Processing, Volume 38, pp. 979-990, 1990.

[10] Wong, P.W., "Fully Sigma-Delta Modulation Encoded FIR Filters", IEEE Transactions on Signal Processing, Volume 40, pp. 1605-1610, 1992.

[11] Memon, T.D., Beckett, P., and Sadik, A.Z., "Efficient Implementation of Ternary SDM Filters using State-of-the-Art FPGA", Mehran University Research Journal of Engineering and Technology, Volume 30, No. 2, pp. 207-212, Jamshoro, Pakistan, April, 2011.

[12] Memon, T.D., Beckett, P., and Sadik, A.Z., "Power-Area-Performance Characteristics of FPGA-Based Sigma-Delta FIR filters", Journal of Signal Processing Systems, Volume 70, pp. 275-288, 2013.

[13] Memon T.D., and Beckett, P., "The Impact of Alternative Encoding Techniques on Field Programmable Gate Array Implementation of Sigma-Delta Modulated Ternary Finite Impulse Response Filters", Australian Journal of Electrical & Electronics Engineering, Volume 10, pp. 107-116, 2013.

[14] Pathan, A., Memon,T.D., Keerio, S., and Kalwar, I.H., "FPGA Based Performance Analysis of Multiplier Policies for FIR Filter", International Conference onAdvances in Electrical, Electronic and Systems Engineering, pp. 17-20, 2016.

[15] Nair, P.P., John, T.M., and John, K, "Optimized FIR Filter using Distributed Arithmetic Architecture", International Journal of Engineering Research, pp. 184-186, 2017.

[16] Mehboob, R., Khan, S.A.,and Qamar, R., "FIR Filter Design Methodology for Hardware Optimized Implementation", IEEE Transactions on Consumer Electronics, Volume 55, pp. 1669-1673, 2009.

[17] Madhumatke, P., Borkar, S., and Katole, D., "A Survey on Power Reduction Techniques in FIR Filter", International Journal of Computing & Technology, Volume 1, No. 6, July, 2014.

[18] Kumar, D.J., and Logashanmugam, E., "Performance Analysis of FIR Filter Using Booth Multiplier", IEEE International Conference on Current Trends in Engineering and Technology, pp. 414-417, 2014.

[19] Narasimha, A. Rajasekhar, R.K., and Rani, A.S., "Implementation of Low Area and Power Efficient Architectures for Digital FIR Filters", International Journal of Advanced Research in Computer Science and Software Engineering,Volume 2, No. 8, pp. 238-244, August, 2012.

[20] Rashidi, B., Rashidi, B., and Pourormazd, M., "Design and Implementation of Low Power Digital FIR Filter Based on Low Power Multipliers and Adders on Xilinx FPGA", 3rd International Conference on Electronics Computer Technology, Volume 2, pp. 18-22, 2011.

[21] Pathan, A., and Memon, T.D., "An Optimized 3x3 Shift and Add Multiplier on FPGA", 14th International Bhurban Conference on Applied Sciences and Technology, pp. 346-350, 2017.

[22] Kawahito, S., Kameyama, M., and Higuchi, T., "Multiple-Valued Radix-2 Signed-Digit Arithmetic Circuits for High-Performance VLSI Systems", IEEE Journal of Solid-State Circuits, Volume 25, pp. 125-131, 1990.

[23] Chandel, D., Kumawat, G., Lahoty, P., Chandrodaya, V.V., and Sharma, S., "Booth Multiplier: Ease of Multiplication", International Journal of Emerging Technology and Advanced Engineering, Volume 3, pp. 326-330, 2013.

[24] Ramannawar, S., and Kumar, D., "Efficient Multiplier Design Using Modified Booth Algorithm and Razor Flip-Flop", International Journal of Science, Engineering and Technology Research, Volume 6, No. 1, pp.166-169, January, 2017.