Mehran University Research Journal of Engineering and Technology

https://doi.org/10.22581/muet1982.3139

2024, 43(2) 195-204

A novel approach toward optimized image processing using sigma delta modulation

Aneela Pathan [a, *], Tayab D Memon [b, c], Rizwan Aziz [a], Syed Haseeb Shah [a]

[a] *Department of Electronic Engineering, The University of Larkana, Larkana, Pakistan*

[b] *Center for Artificial Intelligence Research and Optimization, Faculty of Design and Creative Technology, Torrens University, Melbourne, Australia*

[c] *Department of Electronic Engineering, Mehran University of Engineering and Technology, Jamshoro, Pakistan*

[*] Corresponding author: Aneela Pathan, Email: pathan_aneela@quest.edu.pk

Received: 02 January 2024, Accepted: 28 March 2024, Published: 01 April 2024

KEYWORDS

Image Processing

MATLAB

SDM

Optimization

Digital Signal Processing

Noise

ABSTRACT

Image processing has widespread uses practically in every branch of science and arts. Processing images is more difficult than processing sound or data as there are more bits in the high pixel quality image. It requires more space to store the image, more bandwidth to transmit it, and more time and resources to process. An image's complexity may decrease if its bit size is decreased. Sigma-delta modulation, or SDM for short, is an alternative method of minimizing data-word length to compression. Digital signal processing (DSP) systems can be made simpler by using the SDM approach, which was first created for analog to digital conversion (ADC). This paper suggests a novel way to use SDM in MATLAB for improved image processing. Consequently, the suggested single-bit SDM-based image arithmetic architecture is tested and compared with the traditional image arithmetic techniques. Additionally, to see the noisy channel influence on the traditional and proposed systems, some statistical metrics are also studied at different noise variance values, such as signal to noise ratio (SNR), mean square error (MSE), and Peak SNR value. The suggested architecture for the SDM-based image arithmetic precisely matches the addition and subtraction results of the conventional design, even yielding a higher SNR and the same Peak SNR as the traditional methods. In contrast, the outcomes of division and multiplication fall within an acceptable range. For better results the over-sampling ratio (OSR), an inherent characteristic of SDM must be increased at the cost of more processing cycles. Therefore, the trade-off between fewer resources, limited transmission bandwidth, and comparatively more cycles is provided by the SDM-based technique.

1. Introduction

Image processing has become very common today [1-3]. We use mobile phones to capture, process, store, and transmit images. It is noticed that the higher the resolution of an image is, the more space would it requires [4]. Also, the transmission of high-resolution images takes more bandwidth. When image processing algorithm is implemented on any hardware, like ASIC (Application Specific Integrated Circuits) or FPGA (Field Programmable Gate Array), the hardware gets saturated [5, 6]. One solution to this is image compression, which, again, is another DSP application. Instead, if the data word length is reduced to single bit, the processing will become easy and fewer resources will be required.

A few decades back, a technique for analogue to digital conversion was introduced, known as sigma-delta modulation [7]. SDM is based on the over sampling by a numeric value in which instead of sending the whole data, the difference between sample values is encoded and transmitted, that hardly takes a single or two bits. With this the noise energy gets distributed over a broader range of higher frequencies [8].

Various SDM-based DSP applications for word length reduction and hence reducing the overall system complexity are reflected in the literature that includes but is not limited to simple arithmetic units [9-11], FIR filters (fully or partially transformed to single-bit) [12-19], IIR filters [20-22], and some complex adaptive filter structures [23-26]. Other recent examples of SDM-based short word length systems include adaptive channel equalizers using a μ-less approach [27], Weiner filters [28], Matched filters [29], digital arithmetic units [30], smart sensor communications [31], correlation-less filters [32, 33] and latest SDM-Based Image Processing [34].

This work is continuation of [34] where the conventional methods of image arithmetic are compared with proposed single-bit SDM-based image arithmetic architectures. Besides, some statistical parameters, including SNR, MSE, and Peak SNR value, at various noise variance values, are also analysed to see the noisy channel effect on the conventional and proposed systems. The results of the proposed architecture of SDM-based image arithmetic track perfectly the results of traditional design in addition and subtraction, even producing better SNR and the same Peak SNR as that of conventional approaches. While for multiplication and division, the results are in an acceptable range. For better results the over-sampling ratio (OSR), an inherent characteristic of SDM must be increased at the cost of more processing cycles. Therefore, the trade-off between fewer resources, limited transmission bandwidth, and comparatively more cycles is provided by the SDM-based technique.

The further distribution of the paper is given as under: In section two, the proposed architecture of SDM-Based Image Arithmetic is given and discussed. Section 3 shows the MATLAB-based simulations of the conventional and proposed architectures; in the last section, the conclusion of the proposed work is presented.

2. Proposed Architecture of SDM-Based RGB Image Arithmetic

RGB image is used as input in general and the processing is done on individual channel (Fig.1) or on whole image (Fig.2)

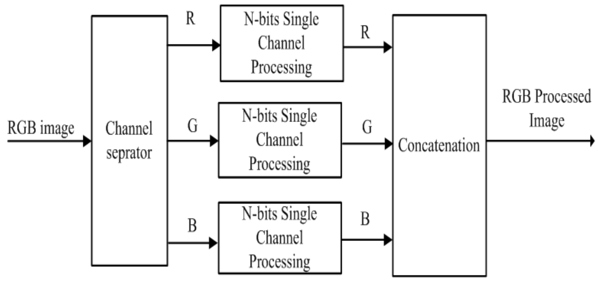

Fig. 1. Traditional Separated Channel Image Processing Architecture [34]

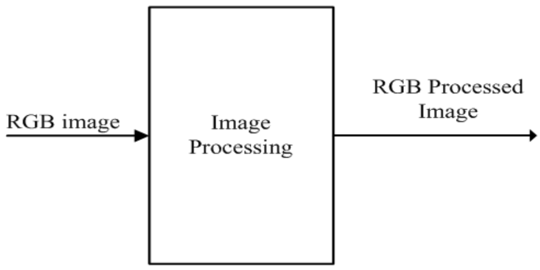

Fig. 2. Traditional Image Processing Architecture [34]

Multi-bit image processing requires more processing time and resources because of the large size of the image. Once the image is converted to a single-bit format using SDM, it will have a significant impact on the resources consumed. Fig.3 illustrates the architecture of single-bit SDM-based image processing and demonstrates how SDM can be used with RGB images. It can be used on practically any kind of image, including binary, colorful, and grayscale ones.

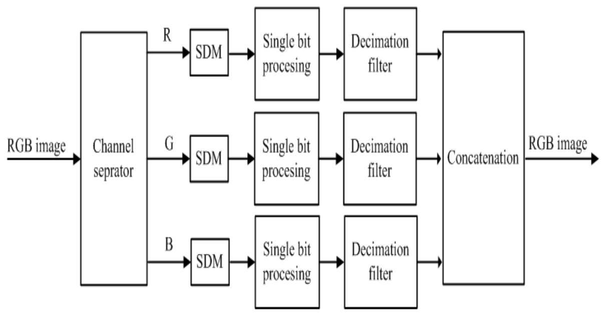

Fig. 3. Proposed SDM -Based Single-Bit Image Processing Architecture

In the proposed design, each color (channel) is separated using the separator block and is passed through SDM. The SDM contains the OSR block. The OSR increases the total sample count according to the principle of Eq. (1). For every image processing step, every sample is transferred to a single bit processing block.

$$\text{No: of Samples} = \text{Origional Samples X OSR} \quad (1)$$

Since the OSR increases the sampling rate, the decimation filter is applied at the output to return the sampling rate to its previous level. The processed channels are then combined to form the RGB image.

The transmission of huge images over communication lines is one of the problems. If the image is not compressed before being delivered, a lot of bandwidth will be needed, and occasionally compression causes the quality of the image to deteriorate.

The idea of single-bit image transmission may also be used in this situation. The architecture for transmitting single-bit images across the data transmission channel is depicted in Fig. 4. The image is transformed to three channels, as before (Fig.1), before it enters the SDM block.

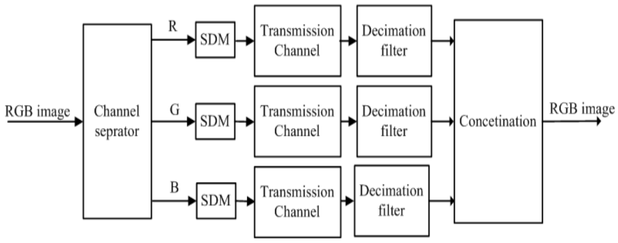

Fig. 4. Proposed SDM-Based Single-Bit Image Transmission Architecture

The SDM block converts the multi-bit image data into single bit, and the OSR increases the data rate by a certain factor. This single-bit data may be sent over any communication channel with reduced bandwidth requirements by a factor of:

$$\frac{1}{\text{Origional Sampling Rate}} \quad (2)$$

Thus one-bit images transmission not only decreases the amount of bandwidth but also avoid other image-related processing steps such as encoding and encryption. Since OSR flattens and reduces the noise floor, its effect is observed in increased SNR of SDM-based images.

Image arithmetic has a main role in image processing. The four main image arithmetic operations include addition, subtraction, multiplication, and division. A general block diagram of image arithmetic is shown in Fig. 5.

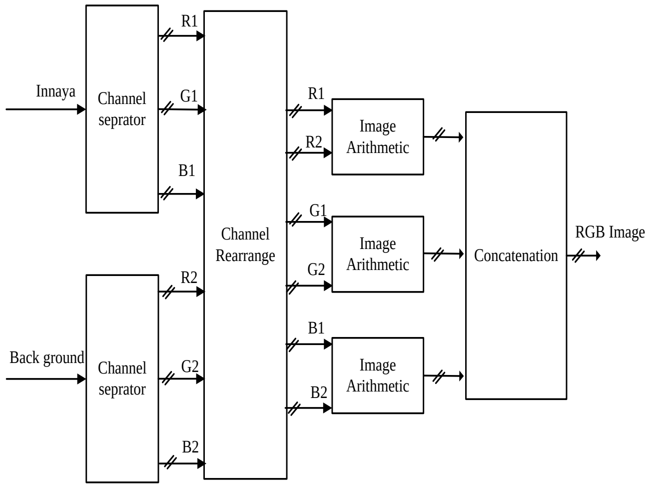

Fig. 5. General Block Diagram of Image Arithmetic

Any of the operations may be performed on an image as whole or on each channel individually. Multi-bit image arithmetic consumes more resources than conventional, but if converted to single bit, the benefits of SDM may become inherent. The architecture of single-bit image arithmetic is proposed in Fig. 6.

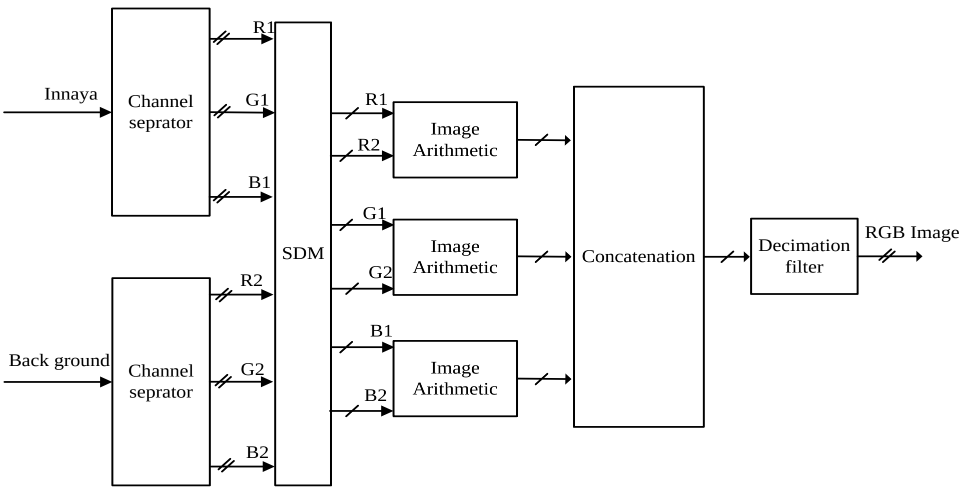

Fig. 6. Proposed Architecture of Single-Bit Image Arithmetic

In the proposed architecture of image arithmetic, two 8-bit images of equal dimensions of 720×720 are given as input. Further, each image is passed through the channel separator block. The channel separator produces six channels, with total bits in individual channels being 720×720×8=4147200. Each channel is passed through an SDM block that contains OSR. After passing through the OSR block with OSR 32, the total number of single bits in each channel would be 132710400. These single bits are then added, subtracted, multiplied, and divided bit by bit, reducing the need for complex multi-bit processing. The results obtained after image arithmetic are produced in the proceeding section, along with an investigation of some characteristic parameters needed to justify using SDM in image arithmetic.

3. MATLAB Based Simulation and Results

An input RGB image of Innaya and a background image (Fig.8-9) of dimensions 720×720 are given to the proposed architecture of image arithmetic (Fig.5-6). Two images are added, subtracted, multiplied, and divided. The results are shown in the preceding section. To check the effect of channel, the salt and paper noise (with different variances) is added to the images and its impact on both approaches is analyzed.

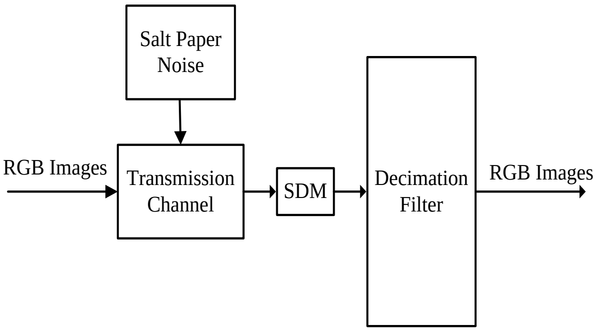

Fig. 7. Salt and Paper Noise Added in Image

Fig. 8. Input Image of Innaya

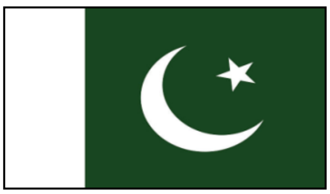

Fig. 9. Background Image

As mentioned above, two images of the same dimensions are given to multi-bit and single-bit arithmetic units (Fig 5-6). The conventional addition of two images produces the result depicted in Fig. 10. Whereas the SDM-based image addition is delivered in Fig. 11. The difference between the two results is shown in Fig. 12. Both the conventional and SDM-based image addition works similarly without much difference.

Fig. 10. Two Images Added with Conventional Arithmetic Addition

Fig. 11. SDM-Based Addition of Images

Fig. 12. Difference Between Conventionally and SDM-Based Added Images

As the salt and paper noise is added to image (Innaya) with different variance values (the noise variance is adjusted over the range 0 to 1, that very approximately ±1 SD from the sample mean), their effect on the image is calculated in terms of SNR, Peak SNR, and MSE. Fig.14 shows that as the noise variance increases, the SNR decreases as it should, but it is worth noting that the SDM-based image addition (shown with blue color) produces better SNR than the original addition of two images (red color).

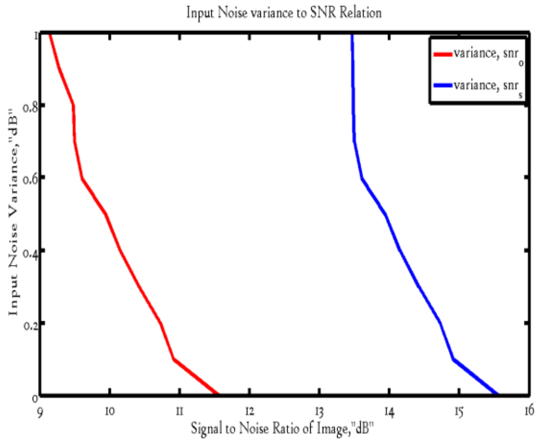

Fig. 13. Noise Variance VS SNR Relation in Addition

Likewise, the Noise variance versus Mean square error is produced in Fig.14. The results show that the change in noise variance does not affect the multi-bit image addition, delivering a constant MSE value, whereas its impact is prominent in single-bit image addition.

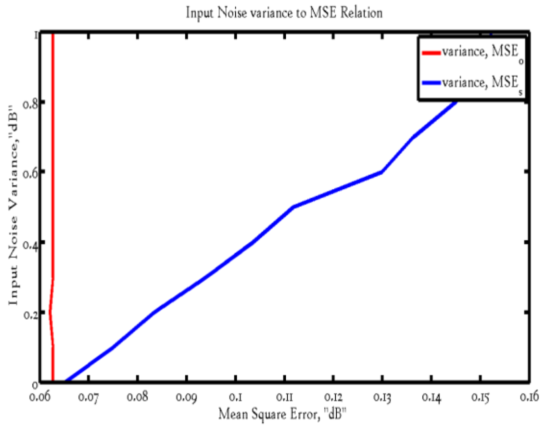

Fig. 14. Noise Variance VS MSE Relation in Addition

A third parameter compared is the Peak signal-to-noise ratio. It may be observed from Fig.15 that the Peak SNR value is the same in both cases (single-bit and multi-bit), hence making the proposed design more acceptable.

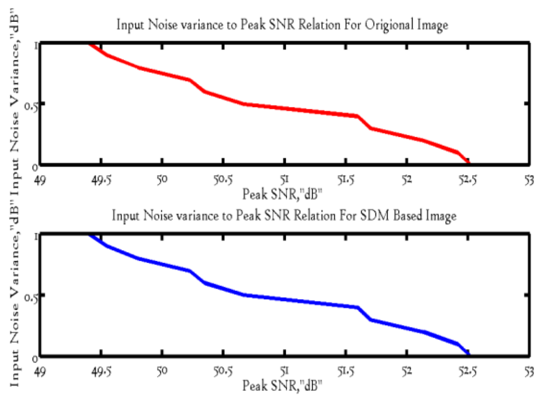

Fig. 15. Noise Variance VS Peak SNR Relation in Addition

The results clearly indicate that SDM based technique works the same as the conventional method and produces a good SNR value because of the over sampling ratio that flattens the noise floor and reduces its impact.

The image subtraction with the conventional method is shown in Fig.16, and the SDM-based result is given in Fig.17.

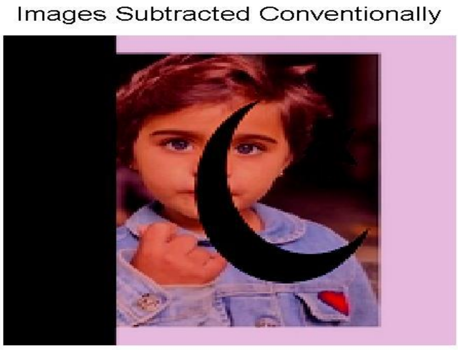

Fig. 16. Two Images Subtracted with Conventional Arithmetic Subtraction

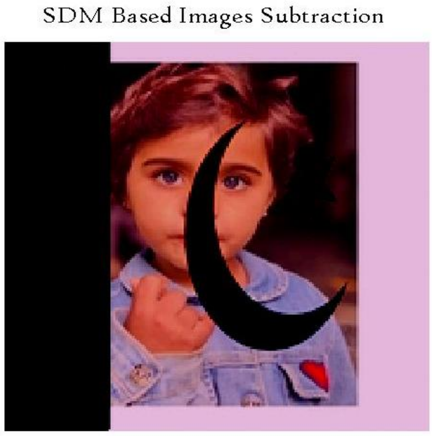

Fig. 17. SDM-Based Subtraction of Two Images

The difference between multi-bit and single-bit image subtraction is given in Fig. 18. Like image addition, single-bit image subtraction produces acceptable results, making it a suitable choice when the resources are of significant concern.

Fig. 18. Difference Between Conventionally and SDM-Based Subtracted Image

The statistical parameters, including SNR, MSE, and Peak SNR, are also compared for both multi-bit and single-bit image subtraction, and the results are given in Fig.19 and Fig.21.

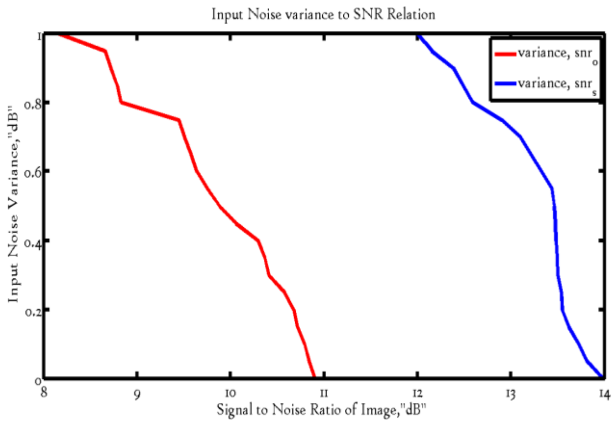

Fig. 19. Noise Variance VS SNR Relation in Subtraction

It may be observed that, similar to addition, the SNR of the proposed design is higher than the conventional design, and as for noise variance, the value increases in the single-bit case and remains constant in multi-bit. But the range in the SDM-based approach is still acceptable.

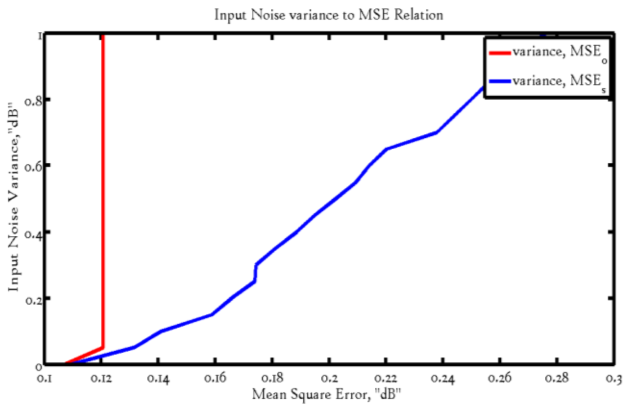

Fig. 20. Noise Variance VS MSE Relation in Subtraction

The noise variance versus Peak SNR for multi-bit and single-bit approaches is shown in Fig.21. As both methods produce the same values, SDM is acceptable as the replacement for the multi-bit process.

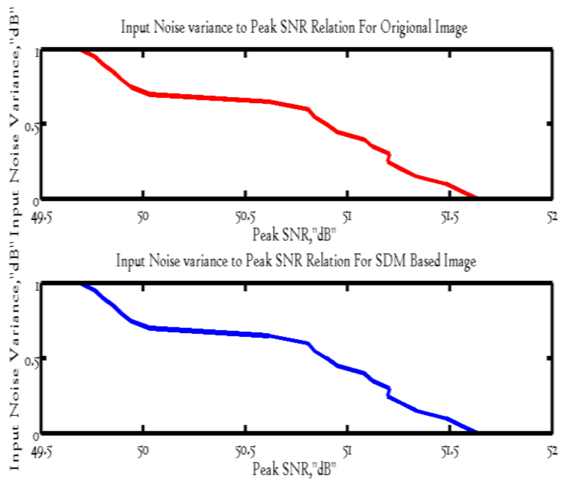

Fig. 21. Noise Variance VS Peak SNR Relation in Subtraction

A third arithmetic operation compared is multiplication. The output of image multiplication with a multi-bit approach is given in Fig. 22 and with SDM based system in Fig. 23, and the difference between multi-bit and single-bit image multiplication is shown in Fig. 24.

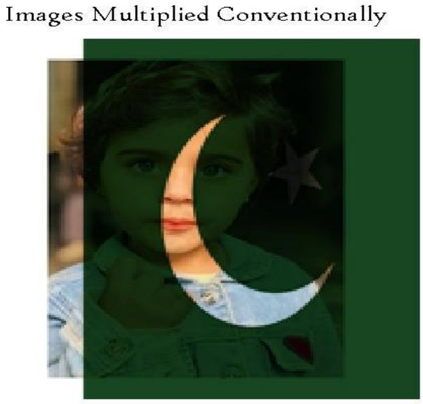

Fig. 22. Two Images Multiplied with Conventional Arithmetic

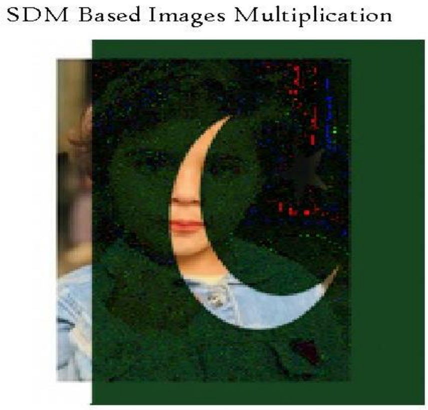

Fig. 23. SDM-Based Multiplication of Two Images

The results of a single-bit multiplier could be better, but still, it may be accepted in various applications immune to errors. The results may get better if the OSR value is increased further. But it is also noticed that increased OSR will increase the time taken to process the data, as the overall data rate may also be increased.

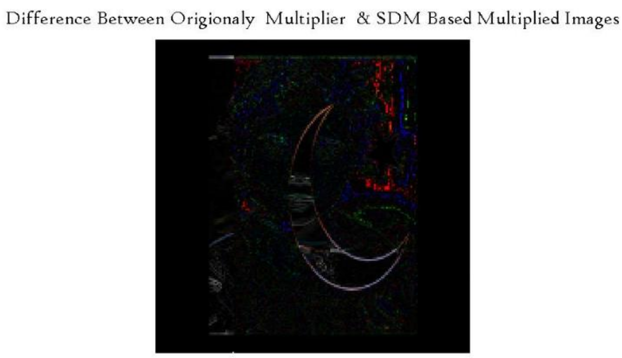

Fig. 24. Difference Between Conventionally and SDM-Based Multiplied Images

The comparison of statistical parameters is shown below. Like in other cases, the SNR value of the SDM-based technique is higher than the conventional multi-bit approach, whereas the MSE of the SDM-based approach is more than the traditional, and the Peak SNR value is the same in both.

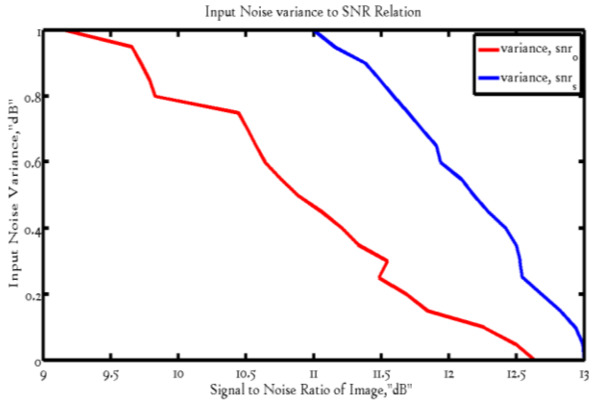

Fig.25. Noise Variance VS SNR Relation in Multiplication

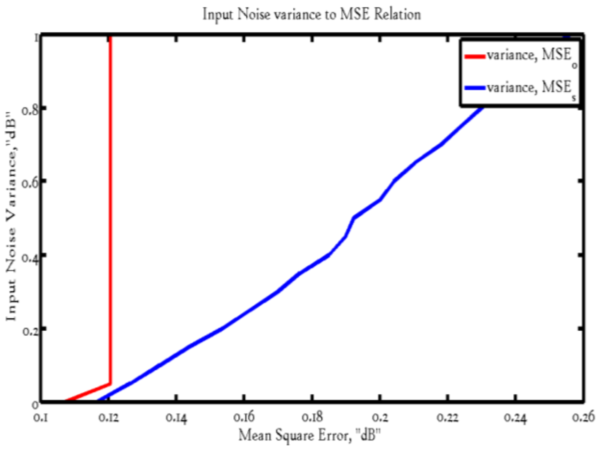

Fig. 26. Noise Variance VS MSE Relation in Multiplication

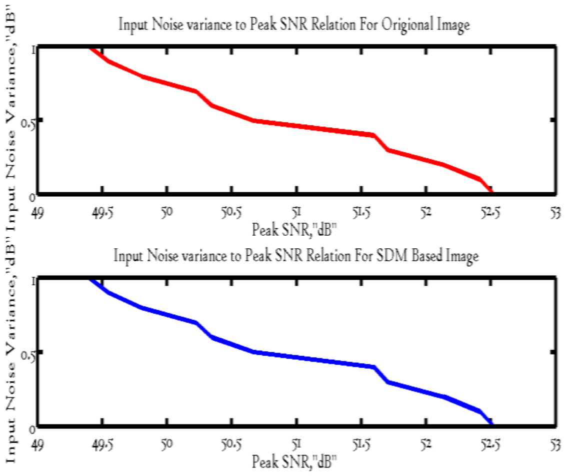

Fig. 27. Noise Variance VS Peak SNR Relation

The last arithmetic operation performed is the division. The results obtained are produced in Fig. 28-30. The multi-bit image division has better results than the single-bit image division. The difference between the two images is also reflected in Fig.30.

Likewise, the statistical parameters are also compared and produced in Fig. 31-33.

Fig.28. Two Images Divided with Conventional Arithmetic

Fig. 29. Two Images Divided with SDM-Based Approach

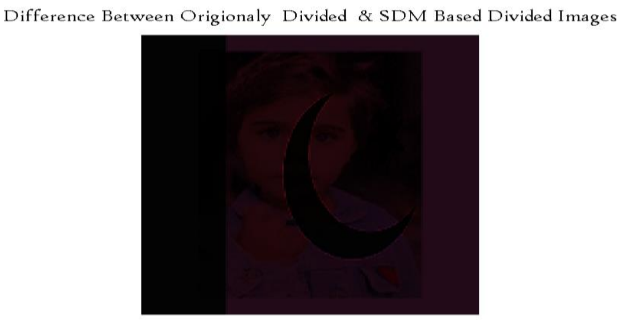

Fig. 30. Difference Between Conventionally and SDM-Based Divided Images

As the results of the SDM-based division are less good than the other three operations, the obtained SNR in the single-bit operation is one dB less than the multi-bit operation that was reversed in the other three operations.

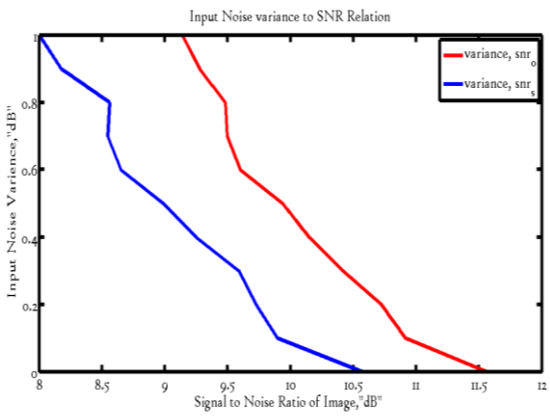

Fig. 31. Noise Variance VS SNR Relation in Division

Fig.32 shows the variance versus MSE graph of both approaches. Like in the other three operations, the conventional process produces the constant MSE value, and in the single-bit method, MSE increases with increased variance. The Peak SNR value in subtraction (Fig.33) also has the same results in both the multi-bit and single-bit approaches.

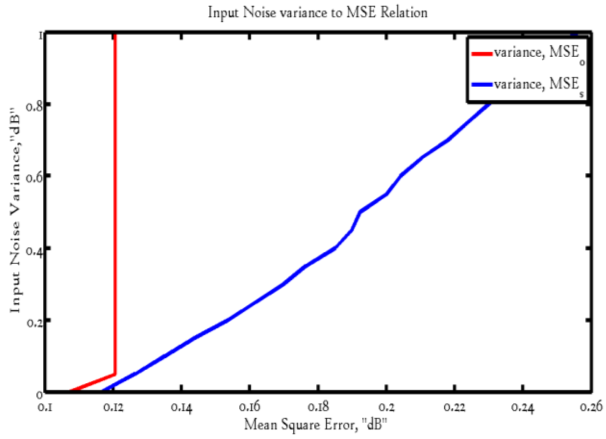

Fig. 32. Noise Variance VS MSE Relation in Division

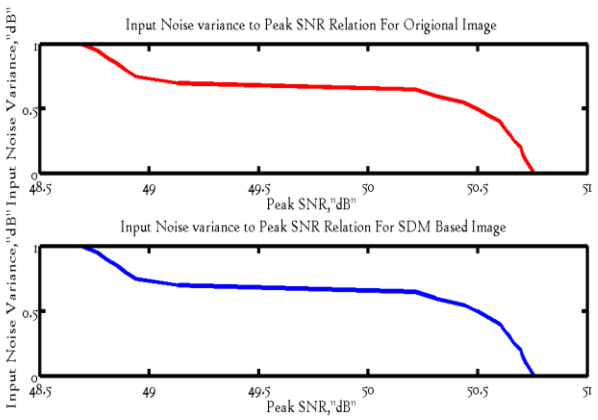

Fig.33. Noise Variance VS Peak SNR Relation in Division

4. Conclusion

A remarkable work in SDM-based signal processing is seen in the literature, while the work in the SDM-based image processing domain is untouched. In this paper, a new trend of applying SDM on images is proposed, discussed, and analyzed by performing image arithmetic. The four arithmetic operations performed here are addition, subtraction, multiplication, and division. Besides, some statistical parameters that include SNR, MSE, and Peak SNR are also calculated and analyzed at different noise variance values.

The statistical parameters indicate that the SNR value of the proposed approach supersedes the conventional method, and the Peak SNR remains the same, while the value of MSE is higher in the proposed approach and constant in the conventional approach.

This increased MSE may be adjusted by growing the OSR in SDM, but it may be one of limiting factor, as the OSR causes the data rate to increase that in turn consumes more processing cycles. Also, an additional block of decimation filter is needed at the receiver end to meet the original data rate.

In the interpolation (OSR) and decimation, some of the actual data is altered that makes the use of this approach limited to less sensitive applications like general video or image processing, and less suited to military and medical applications.

The feasibility of hardware-based single-bit image arithmetic will be analyzed by translating the proposed architecture on FPGAs.

5. References

[1] B. K. Kundu, "THz image processing and its applications", Generation, Detection and Processing of Terahertz Signals, ed: Springer, 2022, pp. 123-137.

[2] Y. Hou, Q. Li, C. Zhang, G. Lu, Z. Ye, Y. Chen, et al., "The state-of-the-art review on applications of intrusive sensing, image processing techniques, and machine learning methods in pavement monitoring and analysis," Engineering, vol. 7, pp. 845-856, 2021.

[3] S. Kaur and C. Diwaker, "An image processing techniques for pattern detection in Covid-19," 2021 6th International Conference on Signal Processing, Computing and Control (ISPCC), 2021, pp. 728-735.

[4] M. Adimoolam, A. John, N. Balamurugan, and T. Ananth Kumar, "Green ICT communication, networking and data processing," Green computing in smart cities: Simulation and techniques, ed: Springer, 2021, pp. 95-124.

[5] V. Subramaniam, "Efficient image compression scheme to minimize storage and bus bandwidth requirements," ed: Google Patents, 2012.

[6] E. C. Anderson, "Transmission bandwidth and memory requirements reduction in a portable image capture device by eliminating duplicate image transmissions," ed: Google Patents, 2007.

[7] P. A. Lopes and J. A. B. Gerald, "Low delay short word length sigma delta active noise control," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, pp. 3746-3757, 2021.

[8] W. Chou, P. W. Wong, and R. M. Gray, "Multistage sigma-delta modulation," IEEE Transactions on Information theory, vol. 35, pp. 784-796, 1989.

[9] G. Xiaodan and M. Qiao, "Hardware implementation of radial basis function neural network based on sigma-delta modulation," 2014 9th International Symposium on Communication Systems, Networks & Digital Sign (CSNDSP), 2014, pp. 1049-1053.

[10] H. Fujisaka, T. Kamio, C.-J. Ahn, M. Sakamoto, and K. Haeiwa, "Sorter-based arithmetic circuits for sigma-delta domain signal processing—Part I: Addition, approximate transcendental functions, and log-domain operations," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, pp. 1952-1965, 2012.

[11] H. Fujisaka, M. Sakamoto, C.-J. Ahn, T. Kamio, and K. Haeiwa, "Sorter-based arithmetic circuits for sigma-delta domain signal processing—Part II: Multiplication and algebraic functions," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, pp. 1966-1979, 2012.

[12] P. W. Wong and R. M. Gray, "FIR filters with sigma-delta modulation encoding," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 38, pp. 979-990, 1990.

[13] C. Dick and F. Harris, "FPGA signal processing using sigma-delta modulation," IEEE Signal Processing Magazine, vol. 17, pp. 20-35, 2000.

[14] N. Temenos, A. Vlachos, and P. P. Sotiriadis, "Efficient stochastic computing FIR filtering using sigma-delta modulated signals," Technologies, vol. 10, p. 14, 2022.

[15] P. W. Wong, "Fully sigma-delta modulation encoded FIR filters," IEEE Transactions on Signal Processing, vol. 40, pp. 1605-1610, 1992.

[16] T. Memon, P. Beckett, and A. Z. Sadik, "Sigma-delta modulation based digital filter design techniques in FPGA," International Scholarly Research Notices, vol. 2012, 2012.

[17] T. D. Memon, P. Beckett, and A. Z. Sadik, "Power-area-performance characteristics of FPGA-based sigma-delta fir filters," Journal of Signal Processing Systems, vol. 70, pp. 275-288, 2013.

[18] T. Memon, P. Beckett, and Z. M. Hussain, "Design and implementation of ternary FIR filter using sigma delta modulation," Proc. ISCCC'09, 9–11 October Singapore 2009, pp. 169-173, 2009.

[19] T. D. Memon, P. Beckett, and Z. M. Hussain, "Analysis and design of a ternary FIR filter using sigma delta modulation," 2009 IEEE 13th International Multitopic Conference, 2009, pp. 1-5.

[20] B. Beliczynski, I. Kale, and G. D. Cain, "Approximation of FIR by IIR digital filters: An algorithm based on balanced model reduction," IEEE Transactions on Signal Processing, vol. 40, pp. 532-542, 1992.

[21] D. A. Johns and D. M. Lewis, "Design and analysis of delta-sigma based IIR filters," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 40, pp. 233-240, 1993.

[22] D. Johns and D. Lewis, "IIR filtering on sigma-delta modulated signals," Electronics letters, vol. 4, pp. 307-308, 1991.

[23] A. Z. Sadik and Z. M. Hussain, "Short word-length LMS filtering," 2007 9th International symposium on signal processing and its applications, 2007, pp. 1-4.

[24] G. Cai, J. Yang, C. Liang, and H. Li, "Design and implementation of LMS adaptive filter algorithm based on FPGA,"2013 2nd International Symposium on Instrumentation and Measurement, Sensor Network and Automation (IMSNA), 2013, pp. 383-385.

[25] T. Memon, P. Beckett, A. Sadik, and P. O'Shea, "Single-bit adaptive channel equalization for narrowband signals," TENCON 2011, pp. 398-402, 2011.

[26] A. Z. Sadik, Z. M. Hussain, and P. O'Shea, "Adaptive algorithm for ternary filtering," Electronics Letters, vol. 42, pp. 420-421, 2006.

[27] T. D. Memon and A. Pathan, "An approach to LUT based multiplier for short word length DSP systems," 2018 International Conference on Signals and Systems (ICSigSys), 2018, pp. 276-280.

[28] A. Pathan, T. D. Memon, F. K. Sohu, and M. A. Rajput, "Analysis of Existing and proposed 3-bit and multi-bit multiplier algorithms for fir filters and adaptive channel equalizers on

FPGA," Quaid-E-Awam University Research Journal of Engineering, Science & Technology, Nawabshah., vol. 19, pp. 81-89, 2021.

[29] A. Chang, T. D. Memon, Z. M. Hussain, I. H. Kalwar, and B. S. Chowdhry, "Design and analysis of single-bit ternary matched filter," Wireless Personal Communications, vol. 106, pp. 1915-1929, 2019.

[30] Y. Liu, P. M. Furth, and W. Tang, "Hardware-efficient delta sigma-based digital signal processing circuits for the internet-of-things," Journal of Low Power Electronics and Applications, vol. 5, pp. 234-256, 2015.

[31] Z. M. Hussain, "Energy-efficient systems for smart sensor communications,"2020 30th International Telecommunication Networks and Applications Conference (ITNAC), 2020, pp. 1-4.

[32] A. Pathan, T. D. Memon, S. Raza, and R. Aziz, "An autocorrelation-less single-bit weiner filter on FPGA," Biomedical Signal Processing and Control, vol. 86, p. 105166, 2023.

[33] A. Pathan, T. D. Memon, and R. A. Mangi, "A correlation-less approach toward the steepest-descent-based adaptive channel equalizer," Circuits, Systems, and Signal Processing, pp. 1-13, 2023.

[34] A. Pathan, T. D. Memon, S. Raza, and R. A. Mangi, "Computationally efficient low-power sigma delta modulation-based image processing algorithm," Mehran University Research Journal Of Engineering & Technology, vol. 42, pp. 102-109, 2023.