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Computationally efficient low-power sigma delta modulation-based image processing algorithm

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K E Y W O R D S

Sigma-Delta Modulation

Image Processing

Low-Power

Power-Efficient

Artificial Intelligence

A B S T R A C T

Digital Image Processing has dominated Digital Signal Processing at the cost of more memory, resources, and high computational power. In image processing, filtering transformations and other operations need complex multiplications, and the multiplier is one of the most resources consuming elements. Recently, mitigating the multiplier complexity in the digital signal processing (DSP) algorithms sigma-delta modulation based general purpose and adaptive DSP algorithms are developed in MATLAB and compared with its counterpart multi-bit algorithms for functionality and area-performance-power in FPGA. The contemporary multiplier algorithms are also optimized to overcome the multiplier complexity challenge as computation becomes simple and fast. This paper extends the reported work by investigating the sigma-delta modulation approaches for developing a computationally efficient low-power image processing algorithm. The proposed model is designed, developed, and simulated in MATLAB. The simulation results are analyzed using SNR, MSE, and Peak SNR. The simulation results show that the proposed system can better mitigate the noise effect, making it robust for noisy environment.

1. Introduction

Image processing has various applications in diversified science fields [1-3]. The images are often captured, processed, stored, and transmitted [4]. The image takes sufficient memory, substantial computational resources, and power [5, 6].

In image processing, filtering transformations and other operations need complex multiplications, and the multiplier is one of the most resources consuming elements [7, 8]. The research proposes various traditional and nontraditional multiplier optimization methods and schemes and implements software based or on hardware (ASICS and FPGAs) [9-13].

As image transmission requires high bandwidth and energy, the telecommunication companies must minimize the bandwidth and energy footprint of media transmissions and reduce the ever-increasing traffic load due to multimedia traffic [14].

The traditional method to reduce the bandwidth is compression, which is also reported in recent literature [15-17]. The main goal of the compression technique is to eliminate the redundancy of image data so that the digital image will be stored and transmitted more effectively.

Semantic communication has also gained the attention of industries and researchers as it permits to go beyond Shannon's capacity limit in bandwidth-limited communication channels. The objective is to deliver the semantic meaning of the message and not the exact form of the message by sharing a common, prior knowledge and a semantically encoded message, which is expected to perform better than state-of-the-art compression techniques, thereby drastically reducing the physical bandwidth requirement between the transmitter and receiver [18-21].

In image transmission, systems adopt separate channel coding and source coding, where the length of the codeword needs to be (infinitely) long [22]. Thus, using joint source-channel coding (JSCC) can enable significant gains. Joint source-channel coding is the encoding of a redundant information source for transmission over a noisy channel and the corresponding decoding, using a single code instead of the more conventional steps of source coding followed by channel coding. Deep learning has also been extended to JSCC systems for wireless image transmission to perform better than separated source and channel coding [17, 23-25].

Though the deep learning approaches may achieve substantially better accuracy; however this jump comes at the cost of billions of additional math operations and an increased requirement for processing power. In this case, the SDM-based short-word-length image processing algorithms can reduce the overall processing of deep learning models and give better results regarding computation time, processing power, and floor chip area requirements [26].

Generally, SDM, like PCM, was initially introduced for analog to digital conversion [27], but since the '70s, it has diversified its application domain toward data length reduction. The SDM converts the multi-bit data into single-bit (stream of bits); hence, the single-bit data is processed. The benefits of SDM include but are not limited to low cost due to less complicated implementation and no digital multipliers, which results in reduced chip area requirement and low computational power.

Some of the SDM-based DSP systems include FIR filters [28], IIR filters [29], Matched filters [30], Digital Arithmetic Units [31], Adaptive filters [32-35], and Smart Sensor Communications [36].

Recent research demonstrates that the SDM reduces the word length and improves the system's overall quality [37].

To the best of our knowledge, the applications of SDM are still prominent in single-dimensional voice or data signals; its use in multi-dimensional images has yet to be investigated.

This paper proposes an SDM-based architecture of multi-dimensional image processing. It investigates the transmission of SDM-based images in a noisy environment to validate the acceptance of SDM in the new digital image processing domain.

The proposed system is designed, developed, and simulated in MATLAB, which may be carried out for hardware synthesis and its functional verification on a suitable platform like FPGA. The simulation results are further evaluated based on performance parameters, including signal-to-noise ratio (SNR), means squared error (MSE), and Peak SNR. The simulation results show that the proposed sigma-delta modulation-based image processing system offers comparable results and observes less effect of noise. This result makes the proposed design very suitable for noisy environment.

The rest of the paper proceeds as follows. An introduction to sigma-delta modulation is given in section 2, followed by the proposed single-bit SDM-based image processing and transmission system in section 3. In section 4, the proposed design is simulated, and the results are compared with the contemporary multi-bit image transmission system. Section 5 concludes the paper, followed by the point to the future work.

2. Sigma-Delta Modulation (Σ-Δ ADC)

The analog to digital converters can be divided into two categories depending on the sampling ratio. The first category is the Nyquist rate ADCs, in which the input data is sampled at the Nyquist rate, and the second type, an oversampling ADCs, samples the signal at a rate much higher than the Nyquist rate. Sigma-delta modulators (Fig.1) come under the over-sampling converters (by oversampling, the sampling frequency is increased by a factor, k, and the noise energy is distributed over a broader range of frequencies) [38].

The transmission efficiency of SDM based system is higher, as instead of sending full data values, only the changes (delta) in value between consecutive samples are transmitted.

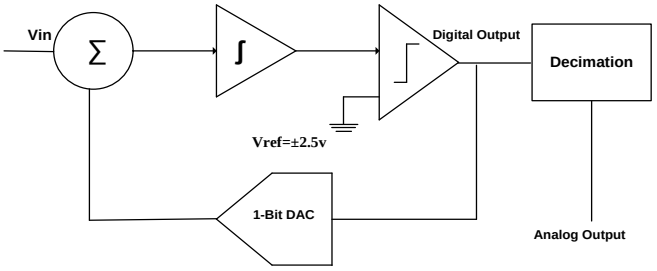

Fig. 1. Sigma-delta modulator

The Sigma-delta modulator design of Fig. 1 consists of a summing node, an integrator, a comparator, and a D/A converter. The first block is the difference block (summing note) to which analogue input is applied, and from it, the feedback signal (DAC output) is subtracted. The proceeding block is the integrator that stores the difference. The comparator block works on the output of the integrator where the reference signal is already available. The reference voltage levels are compared with the integrator's output, generating a "high" or "low" value. In turn, the DAC uses the result of the ADC and develops one of the two available reference voltages. This reference voltage is passed to the difference block to be subtracted from the input again. Moreover, in the last, one-bit (high/low) data samples are decimated (down-sampled) by the digital filter to achieve the same data rate when reconverted into an analog.

The output voltage at various blocks of sigma-delta ADC is given in Table 1 for one-volt analog input and 2.5 volts as a reference voltage.

Table 1

Output voltages at various blocks of sigma-delta ADC

Output voltage				
Vin =1	Difference block (Summing Node)	Integrator output	Comp-arator	DAC
	1	1	H	2.5
	1-(2.5)=--1.5	1+(-1.5)=--0.5	L	-2.5
	1-(-2.5)=3.5	(-0.5+3.5)=3	H	2.5
	1-(2.5)=--1.5	3+(-1.5)=1.5	H	2.5
	1-(2.5)=--1.5	1.5+(-1.5)=0	H	2.5
	1-(2.5)=--1.5	0+(-1.5)=--1.5	L	-2.5
	1-(-2.5)=3.5	-1.5+(3.5)=2	H	2.5
	1-(2.5)=--1.5	2+(-1.5)=0.5	H	2.5

3. Proposed Architecture of SDM-Based Image Processing

Conventional image processing takes the RGB input image and performs the required processing on the individual channels(Fig.2), or on the image as a whole (Fig.3).

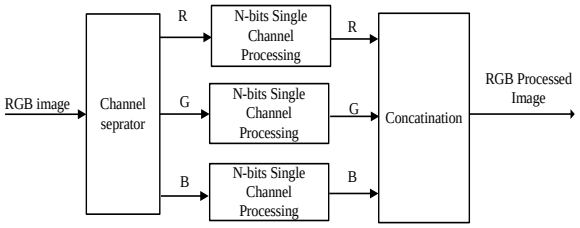

Fig. 2. Conventional architecture of separated channel image processing

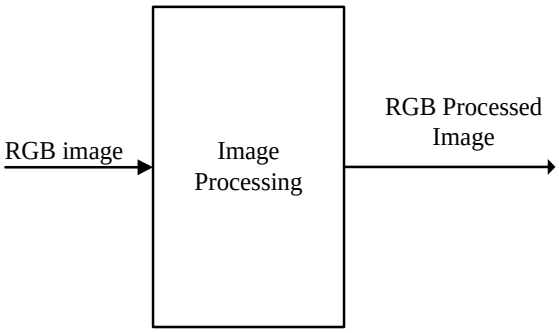

Fig. 3. Conventional architecture image processing as a whole

The proposed architecture for SDM-based single-bit image processing is shown in Fig.4, which depicts how the SDM technique can be applied to an RGB image. It is generally possible to apply it to any image, including grey, binary, or colored images.

For the case of RGB images, the SDM technique is applied individually on each color by separating it with the help of a separator block in MATLAB. Each eight-bit color channel is then passed through SDM for converting the multi-bits to a single bit. The SDM block contains the over-sampling ratio (OSR) that causes the increase in the total number of samples as per the principle shown in equation (1).

$$\text{Number of Samples} = \text{Original Samples} \times \text{OSR} \quad (1)$$

All the samples are then moved to a single-bit processing block for performing any image processing operation.

Since the sampling rate has been increased with the OSR ratio, applying a decimation filter at the output becomes mandatory to bring the rate to its original value.

The different channels of the processed image are then concatenated to produce the same RGB image.

In the proposed design, the dimensions of the input image are 720×720, where each pixel is 8-bit wide. The total bits in individual channels are 720×720×8=4147200, and after passing through the OSR block with OSR 32, the total number of single bits would be 132710400. This single-bit can now be transmitted on the channel or easily processed with simple gates.

One of the significant constraints of the proposed design is the total number of cycles consumed. As the SDM-based approach has oversampling ratio and with increased OSR data rate increases. The increased data rate cause more processing time while with less resource consumption.

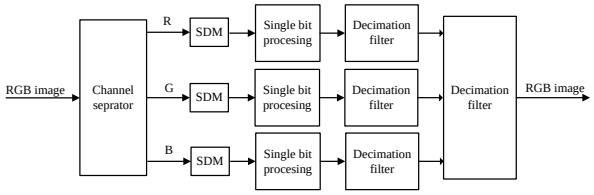

Fig. 4. Proposed architecture for SDM based single bit image processing

Fig. 5 shows the architecture of single-bit image transmission over the data transmission channel. As shown in Fig.4, the image is converted to three different channels before passing through the SDM block.

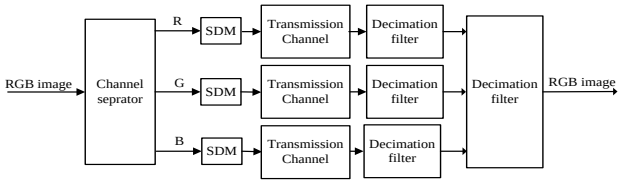

Fig. 5. Proposed architecture for SDM based single bit image transmission

The SDM block causes the OSR to work here and increases the total single-bit samples. The single-bit samples can then be transmitted over any communication channel by reducing the total bandwidth requirement by the factor of:

1/Original Data Rate (2)

.

To produce the impact of the channel in real-time, the salt and paper noise with a range of variance values is added, and number of simulations is carried out. The noisy image is passed to the decimation filter then to convert the single-bit SDM-based filter to back in multi-bit. The data rate increased with OSR has now been reduced to its original value.

This single-bit transmission of the image not only reduces the bandwidth but also helps in getting rid of other image-related processing, like encoding or encryption.

As the OSR causes the noise floor to be flattened and reduced, the effect may be observed in SDM-based images in increased SNR.

4. MATLAB-Based Simulations and Results

An input RGB image of Innaya (Fig.6) of dimensions 720×720 is given to the channel separator block for getting separate Red, Green, and Blue channels.

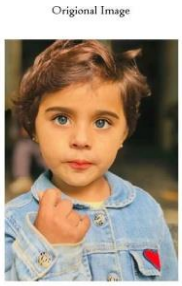

Fig. 6. The input RGB image of Innaya for single-bit transmission

To check the effect of noise supposed to be included while transmission, the prevalent salt and paper noise with different variance values is added to the image.

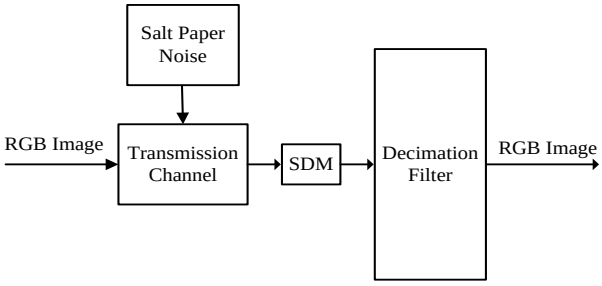

Fig. 7. Salt Paper noise added image

Each RGB channel is moved to the SDM block, where the OSR cause the data rate to be increased by a factor of 32. No further image compression or channel coding is applied, while at the receiver decimation filter is used to return the data rate to its original value.

Fig. 8 shows the SDM-based single-bit image, reconstructed by applying a decimation filter and combining the separate channels to get the same RGB image.

While observing the two (Fig.7-8), it is clear that SDM brings no generic effect on the original image, and

the reconstructed image is the replica of the original input image. The original and SDM-based image is then compared to see the difference between the two.

A tow dimensional error matrix is generated when the reconstructed image is subtracted from the original image. The produced result is presented in Fig. 9.

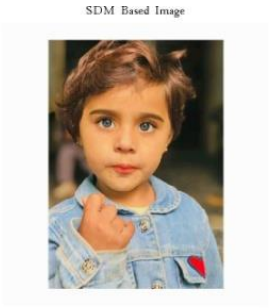

Fig. 8.SDM based single bit transmitted and reconstructed image of Innaya

Fig. 9. Difference between the original and SDM-based images of Innaya

The advantage of oversampling in delta-sigma modulation is that the noises are spread over a more extensive frequency range, reducing the noise spectral density that in turn causes the SDM systems to be more immune to noise.

The proposed architecture was further investigated to verify the concept by looking into some performance parameters like signal-to-noise ratio, mean square error, and peak signal-to-noise ratio at a range of noise variance values.

As the signal-to-noise ratio and the mean square error are inversely proportional to the noise variance, the same results are observed in simulations with a conspicuous point that due to OSR in SDM, less effect of variance is observed on SDM-based image.

Fig. 10 shows the graph of input noise variance to SNR relation for both the input and SDM-based images. The values of both parameters are taken into dB.

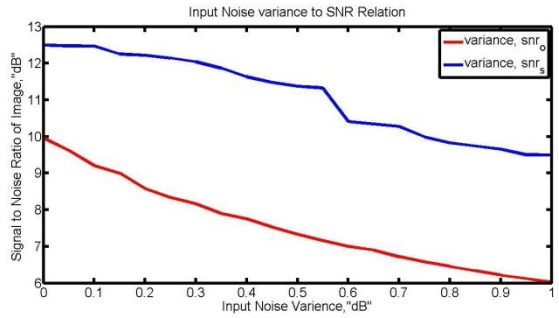

Fig. 10. Input noise variance to SNR relation

It may be observed from the variance to SNR relation that in comparison to the original image, the SNR of the SDM-based image observes less effect of input noise variance, and hence in a noisy environment SDM may play a vital role.

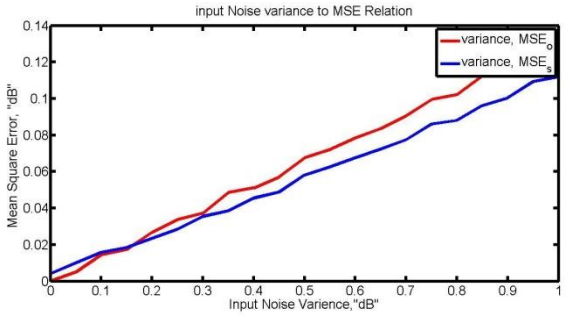

Fig. 11. Input noise variance to MSE relation

Another performance parameter considered is the mean square error. The graph in Fig.11 shows that for SDM-based images less mean square error is observed than the original input image.

The peak SNR to noise variance graph is shown in Fig.12. Like the other two parameters, the SDM-based image shows more Peak SNR value for SDM-based image resulting in the reconstruction of the degraded image even better than the original image.

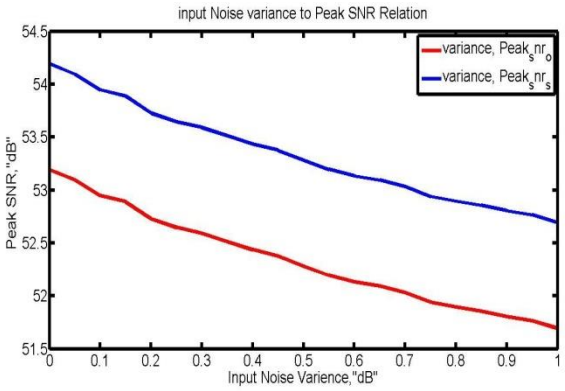

Fig. 12. Input noise variance to Peak SNR relation

5. Conclusion and Future Work

Since its exceptional use, sigma-delta modulation has diversified the digital signal processing domain by incorporating features like the oversampling ratio. With

increased OSR, the SNR, Peak SNR, MSE, and other performance parameters are improved, making the overall processing much more straightforward and reducing the power requirements.

In this paper, the SDM is applied to a multi-bit RGB image for its single-bit transmission, and its various performance matrices are observed and analyzed to see if the SDM may be used in this new domain of single-bit image processing. Besides, the proposed architecture of single-bit image processing is also discussed in detail.

The various simulation results demonstrate the importance of SDM and open the doors of its use in the image processing domain, which could drastically reduce the bandwidth requirements for the transmission of digital images.

In the future, the SDM will be investigated and applied to various image processing algorithms for image filtration and enhancement, along with its hardware-based implementation on FPGAs; while it is assumed that the images are digital and in the format that an FPGA may process. Besides, the applications for SDM-based image processing would be more generic and may accept some loss of information rather than bio-medical image processing or more sensitive fields.

6. Acknowledgement

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