Medium Voltage Three Phase Static Transfer Switch Operation: Simulation and Modeling

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ABSTRACT

In this paper, comparison of control logic based on delay logic technique and forced commutation technique for thyristor based three phase medium voltage STS (Static Transfer Switch) has been made. The developed forced commutation technique for thyristor based STS has broadens the scope of applications in utility distribution network for implementation of different demand side management options. Most importantly, forced commutation technique has shown significant performance for loads having variable power factor. Different point-on-wave with a span of 18° and time duration of 0.001 second has been simulated using delay-logic and forced commutation based control logic techniques. PSCAD/EMTDC software has been used for simulation of different case studies.

Key Words: **Cross Current, Forced Commutation, Load Types, Power Distribution System, Sensitive Loads, STS, Transfer Time, Three Phase-to-Ground Fault.**

1. INTRODUCTION

STSs may be used in power distribution system for different applications to enhance the performance and efficiency of the system. These applications include fault isolation, standby power source, switching between preferred and alternate source and/or feeders, exchange of power between electric utilities, and load sharing of heavily loaded preferred feeder with lightly loaded alternate feeder. Use of STS can reduce the distribution system losses and will allow flexible operation of the distribution system. Static transfer switch through the control logic can transfer the load in less than a quarter of the rated frequency cycle [1]. Sensitive loads are usually fed from two independent power sources, preferred and alternate, through the STS to supply uninterruptible power to the load, as shown in Fig. 1. If preferred source fails due to fault or voltage sag then the sensitive load must be transferred to the alternate source through the operation of STS system.

The role of STS control logic is very crucial in implementation of load transfer between the complementary distribution feeders to offset their overloading and under loading effects. None of the available control strategy [2-19] can show significant performance for implementation of STS to transfer the load of a heavily loaded feeder to lightly loaded feeder and vice versa. The control logic of

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the STS system discussed and implemented in [20-21], transfers the load of the preferred feeder to the alternate feeder with no source paralleling and then back to the preferred feeder. Further more the transfer time of the proposed STS's control logic is within permissible limits as laid down in IEEE Std. 446 [22].

When fault or voltage sag occurs on the preferred feeder then control logic generates low gating pulse for the STS-Block-I thyristors and high gating pulse for the STS-Block-II thyristors. As a result the STS-Block-I thyristors are turned off at zero crossing of current and STS-Block-II thyristors are ON and load is now transferred to the alternate feeder. But this is not true to consider that the outgoing thyristors are turned-off at once simply by removing the high gating pulse by the natural commutation of the thyristor of STS-Block-I and load is transferred to the alternate feeder by just applying high gating pulse to the STS-Block-II thyristors. However, the turning-off of the outgoing thyristors of STS-block-I depends on the load power factor. The thyristors of the STS-Block-I are conducting until the zero crossing of current occur and the incoming thyristors of STS-Block-II only be given high gating signal to turn them ON. If STS-block-I thyristors are not fully turned off and thyristors of STS-Block-II are turned on, then the both sources become parallel and the phenomena of cross current occur. To overcome cross current phenomena, it is utmost important that before turning on the incoming thyristors of STS-Block-II, thyristors of STS-Block-I should be turned off completely. Now there are two different approaches to avoid the cross current phenomenon. Mokthari and his colleagues have proposed delay logic approach. In this approach, the firing of the thyristors of STS-Block-II is delayed until the thyristors of the STS-Block-I are completely turned off through natural commutation. This approach is, as will be described later, not capable for fast transfer of loads having varying power factor between two feeders and also if input voltages at the PoI of STS are not in-phase [6]. Thyristor switching time through natural commutation increases as load power factor changes. So it becomes difficult to determine the exact delay time after which the incoming thyristors are fired to transfer the load from the preferred feeder to the alternate feeder. The second approach is called the forced commutation technique. This technique is most suitable for STS-system operation as compared to the delay logic technique. This technique is explained in the later section of the paper and different simulation cases were run to implement both of the stated approaches using the PSCAD/EMTDC software [23-24]. Different points on the wave have been studied which shows that forced commutation technique is suitable for the STS-system operation.

2. LOAD POWER FACTOR AND STS

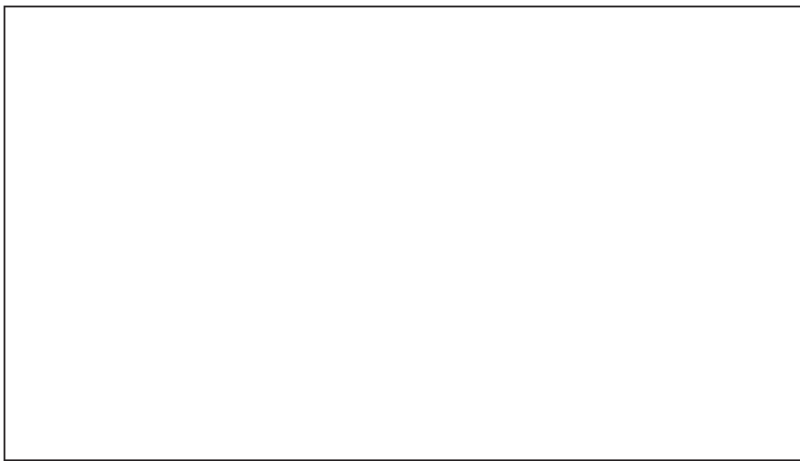

FIG. 1. SCHEMATIC DIAGRAM OF PREFERRED AND ALTERNATE FEEDER WITH NORMAL, SENSITIVE LOAD AND STS BLOCKS

OPERATION

The main purpose for the installation of STS in the distribution network is to provide uninterruptible power to the sensitive load. However, when the sensitive load demand is constant and hence its power factor is also constant, then the operation of the STS's control logic for transferring of load from the preferred feeder to the alternate feeder and vice versa is some what simple. In case of fixed power factor, a fixed delay in the firing pulse of incoming thyristors will serve the purpose and transfer of load from preferred feeder to alternate feeder will take place without any cross current. However, the situation is complicated in case of varying load, due to variation in the power factor. It becomes difficult to predict the amount of delay in the firing pulse in real time for the thyristors of STS blocks. Following two techniques are used in the STS's control logic to avoid cross current phenomenon in STS blocks of incoming and outgoing feeders.

(a) Delay Logic Technique
(b) Forced Commutation Technique.

2.1 Delay Logic Technique

Many researchers have implemented delay logic technique for fast and safe transfer of the critical load from preferred feeder to the alternate feeder. For some practical applications the delay logic experiences the operational problems in the STS. The cross current phenomenon and source paralleling is an important concern during the transfer operation of the STS. Some researchers have tested the delay logic technique for STS system on IEEE Benchmark system and have shown different simulation results for different types of loads. The STS transfer time for this technique varies in response to different disturbance applications i.e. different fault types and voltage sag. The simulation results of these researchers show that transfer time is variable, and it depends on type of faults and load types. They have concluded that the transfer time with this technique is quite unpredictable for different load and disturbance types. A variation in transfer time in itself is an indication that the delay time introduced in the firing pulse to the incoming thyristor is changing all the time with changes in the load power factor. The firing of incoming thyristor is delayed until the current through outgoing thyristor is at zero crossing.

In Fig. 2 two independent three phase voltage sources or feeders, preferred and alternate feeder, are shown. STS-system consists of STS-Blocks namely STS-Block-I and STS-Block-II and control-logic-block. STS-Block-I is connected in series with the sensitive load and the preferred feeder and is normally ON. Whereas, STS-Block-II is connected in parallel between the alternate feeder and the sensitive load and is normally OFF. Each STS-Block has two thyristors per phase to allow positive and negative half cycle of current to the load. The control logic of the STS-system introduces delay in the firing pulse for the two thyristor blocks. Also, the control logic keeps track the RMS value of the voltage for both the feeders at the PoI (Point of Installation) of STS. In case of any disturbance on the preferred feeder, the control logic generates high gating pulse for the thyristors of STS-Block-II to turn them ON and low gating pulse for the thyristors of STS-Block-I to turn them OFF. Delay logic technique introduces an appropriate delay in the firing pulse to the thyristors of STS-Block-II. When disturbance on the preferred feeder is removed then the control logic generates high gating pulse for the thyristors of the STS-Block-I and transfers the load to the preferred feeder.

2.1.1 Control Logic Block

The control logic block implements the delay logic technique. It consists of the voltage detection logic, main thyristor monitoring and delay logic block.

2.1.1.1 Voltage Detection Logic

The voltage detection logic detects fault or disturbance at preferred feeder at the PoI of STS and removes gating pulse of thyristors for STS-Block-I. The voltage detection circuit, as shown in Fig. 3, compares the RMS phase voltage from the preferred feeder and the RMS phase voltage from the alternate feeder in the comparator. The output of the comparator block is further compared with a threshold value which is usually 5% of the rated voltage. As long as the output of the comparator block is within the threshold value, the output of the comparator is low. When fault or disturbance occurs then output of the comparator will be high. A switching-delay block is introduced to avoid momentary faults and disturbances. The delay time of the switching-delay block is slightly less than the one fourth of the 50Hz frequency cycle. As soon as the output of the switching-delay block is high, the gating pulse of the main thyristors of the STS-Block-I low. If the fault or disturbance time is greater than delay time of the switching-delay block then transfer signal will be generated.

2.1.1.2 Thyristor Monitoring

FIG. 2. SCHEMATIC DIAGRAM OF PREFERRED AND ALTERNATE FEEDER ALONG WITH STS'S CONTROL LOGIC BLOCK

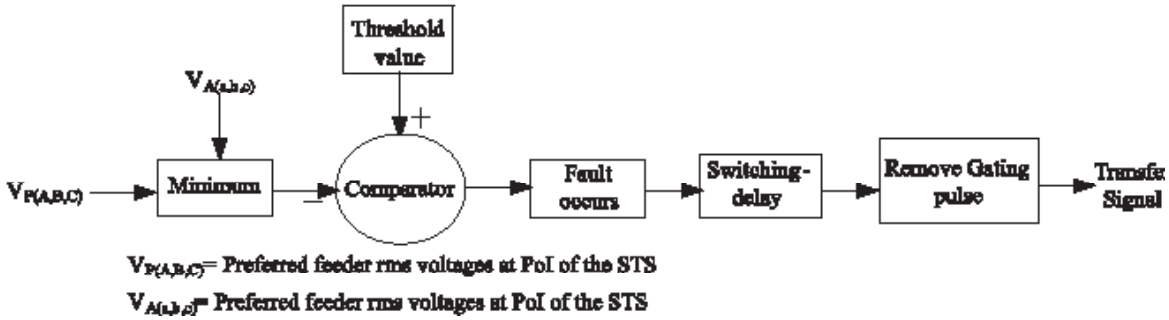

FIG. 3. SCHEMATIC DIAGRAM OF VOLTAGE DETECTION CIRCUIT

The thyristor monitoring logic will generate positive-high signal for positive half conducting main thyristors and negative-low signal for negative conducting main thyristors of STS-Block-I. The output of thyristor monitoring logic is ANDed with the output of the voltage detection block and the resultant output goes to the delay block as control signal as shown in Fig. 4.

2.1.1.3 Delay Logic

The control signal from the thyristor monitoring block recognizes which of the thyristors of STS-Block-I are in conducting mode. The delay logic introduces a delay in the firing pulse of the respective thyristor of STS-Block-II. The delay in the firing pulse of the incoming thyristors is introduced to avoid the cross current phenomena and hence the source paralleling. Sensitive load is now completely transferred to the alternate feeder.

2.2 Forced Commutation Technique

On specific need bases, as described earlier, the STS-system can be used to transfer critical load from the preferred feeder to alternate feeder. The load to be transferred is highly variable in nature; hence the power factor is not fixed. In case of fault or disturbance on the preferred feeder, the control logic of the STS-system must transfer the load served by the preferred feeder to the alternate feeder in minimum possible time. When fault is removed then the control logic of the STS-system must transfer the load back to the preferred feeder. Prior to transfer of the critical load to the alternate feeder, the main thyristors of STS-Block-I should be completely turned-OFF. To turn-OFF the main thyristors of STS-Block-I, the control logic of the STS-system utilizes forced commutation technique. The complete circuit diagram with forced commutation circuit is shown in Fig. 5. In case of fault on the preferred feeder, the control logic of STS-system commutates the main thyristors of STS-block-I through forced commutation and then applies a firing pulse to turn-ON the main thyristors of STS-Block-II. Working of forced commutation technique has been explained in [20]. To avoid complexities in delay time estimation, the forced commutation technique is used for high speed switching of STS for universal applications of the STS-system.

3. SIMULATION AND RESULTS

The STS-system has been consider for different test cases using delay logic technique as well as forced commutation technique for a total simulation time of 0.5 second. Twenty different points-on-wave for one full ac cycle, starting from 0.300-0.320 sec. of the simulation period, are monitored. Each point-on-wave being monitored is 18° apart from the preceding point. The STS system during this period was investigated for three-phase-to ground fault. Two case studies for load types having 0.95 and 0.90 lagging power factors are considered.

Case Study-I: 0.95 Power Factor Lagging

In real world neither the loads are purely resistive nor is the load power factor unity. Most of the loads served by the utility system are inductive in nature hence the power factor is less than unity. It's very important to

FIG. 4. SCHEMATIC DIAGRAM OF THYRISTOR MONITORING BLOCK WITH DELAY LOGIC

consider inductive load for STS operation and then have a comparison between the existing and proposed technique.

The STS-system with preferred and alternate feeder is simulated for RL load having 0.95 power factor lagging. Table 1 shows that cross current occurs while operating STS system at points-on-wave at 0.301, 0.302, 0.303, 0.304, 0.305, 0.306, 0.308, 0.309, 0.311, 0.312, 0.313, 0.314, 0.315, 0.316, 0.318, 0.319 sec. To successfully implement the delay logic technique, firing of the incoming thyristors is delayed by the time as indicated in Table 1. Simulation results show that delay time, in some cases, is not within the permissible limits recommended by relevant standards.

Consider the three-phase-to-ground fault on the preferred feeder at 0.304 sec point-on-wave. The gating pulse of the incoming thyristors of the STS-Block-II is high without making sure commutation of the out going thyristors. Under the circumstances cross current occurs in phase-B as shown in Fig. 6. Fig. 6(a) depicts simulation results of the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}). The transfer time of load-side line-to-ground voltages (VL_{an}, VL_{cn}) is 2ms and is within permissible limits. While that of (VL_{bn}) is 20ms and load served by this phase will face an interruption. Fig. 6(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}). The transfer time for load-side line-to-line voltages (VL_{ab}, VL_{bc}) is maximum and load will be interrupted because voltage sag for VL_{ab} and VL_{bc} is 50% for 20ms which is beyond permissible limit. But the

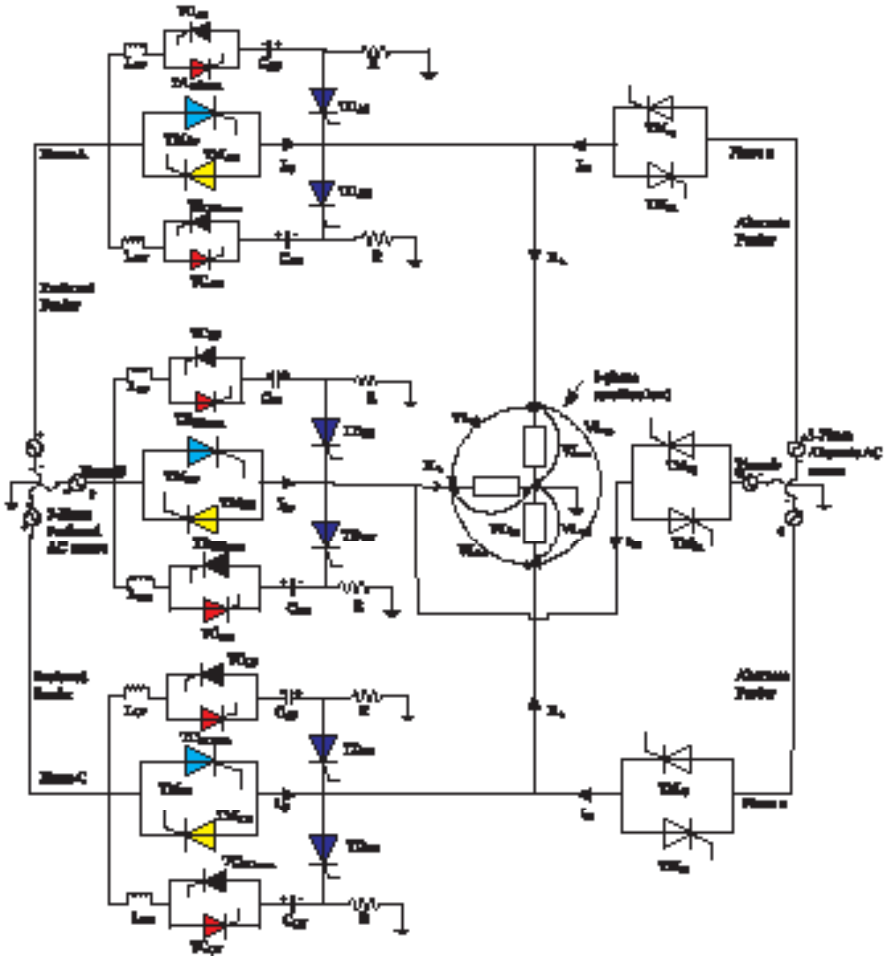

FIG. 5. SCHEMATIC DIAGRAM OF THE PROPOSED COMMUTATION TECHNIQUE IMPLEMENTED FOR THE OPERATION OF STS-SYSTEM FOR 3-PHASE 11 KV DISTRIBUTION FEEDER

transfer time for VL_{ca} is 2ms which is within permissible limits. Fig. 6(c) shows three-phase load-side line currents (IL_a, IL_b, IL_c). Fig. 6(c) shows that the transfer time of line-currents (IL_a, IL_c) is minimium (2ms). But the transfer time of line-current IL_b is maximum (20ms) and hence load interruption for this phase will occur. Fig. 6(d) shows cross current in Phase-B. Hence the source paralleling occurs and the transfer time becomes maximum because the thyristors of STS-Block-II are fired when the companion thyristors of STS-Block-I are still conducting.

To minimize the transfer time, different techniques may be implemented in the control logic of the STS-system. Delay logic is one of these techniques used for the STS-control logic and implemented by some researchers. Simulation results for this technique are shown in Fig. 7. Fig. 7(a) shows the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}). The transfer time of load-side line-to-ground voltages (VL_{an}, VL_{cn}) is 2ms and is within permissible limits. While the transfer time for (VL_{bn}) is 7ms and is beyond the permissible limits. Fig. 7(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}). It shows that the transfer time of load-side line-to-line voltages (VL_{ab}, VL_{ca}) is minimum i.e. 2ms but the transfer time of load-side line-to-line voltage (VL_{bc}) is 4.9ms and is also within permissible limits. Hence load will not experience any source interruption. Fig. 7(c) shows that the transfer time of line-currents (IL_a, IL_c) is minimium and the transfer time for line-current IL_b decreases from 20-4ms. Fig. 7(d) shows that cross current does not occur in the Phase-B of incoming and outgoing STS thyristors. No source paralleling because now the firing of the thyristors of STS-Block-II is delayed until their companion thyristors of STS-Block-I are completely turned-OFF.

TABLE 1. SUMMARY OF SIMULATION RESULTS FOR 0.95 LAGGING POWER FACTOR

No.	Point-On-Wave (Sec)	Occurrence of Cross Current			Delay Time (Incoming Thyristor) (ms)
		Phase-A	Phase-B	Phase-C	
1.	0.300	x	x	x	No Delay Time (No Cross Current)
2.	0.301	x	x	Yes	4.5
3.	0.302	x	x	Yes	3.8
4.	0.303	x	x	Yes	1.8
5.	0.304	x	Yes	x	5.0
6.	0.305	x	Yes	x	4.3
7.	0.306	x	Yes	x	2.7
8.	0.307	x	x	x	No Delay Time
9.	0.308	Yes	x	x	4.3
10.	0.309	Yes	x	x	3.5
11.	0.310	x	x	x	No Delay Time
12.	0.311	x	x	Yes	4.4
13.	0.312	x	x	Yes	3.7
14.	0.313	x	x	Yes	1.7
15.	0.314	x	Yes	x	4.9
16.	0.315	x	Yes	x	4.5
17.	0.316	x	Yes	x	2.8
18.	0.317	x	x	x	No Delay Time
19.	0.318	Yes	x	x	4.3
20.	0.319	Yes	x	x	3.4

FIG. 6. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.95 POWER-FACTOR-LOAD AT THE PREFERRED FEEDER. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) CROSS CURRENT.

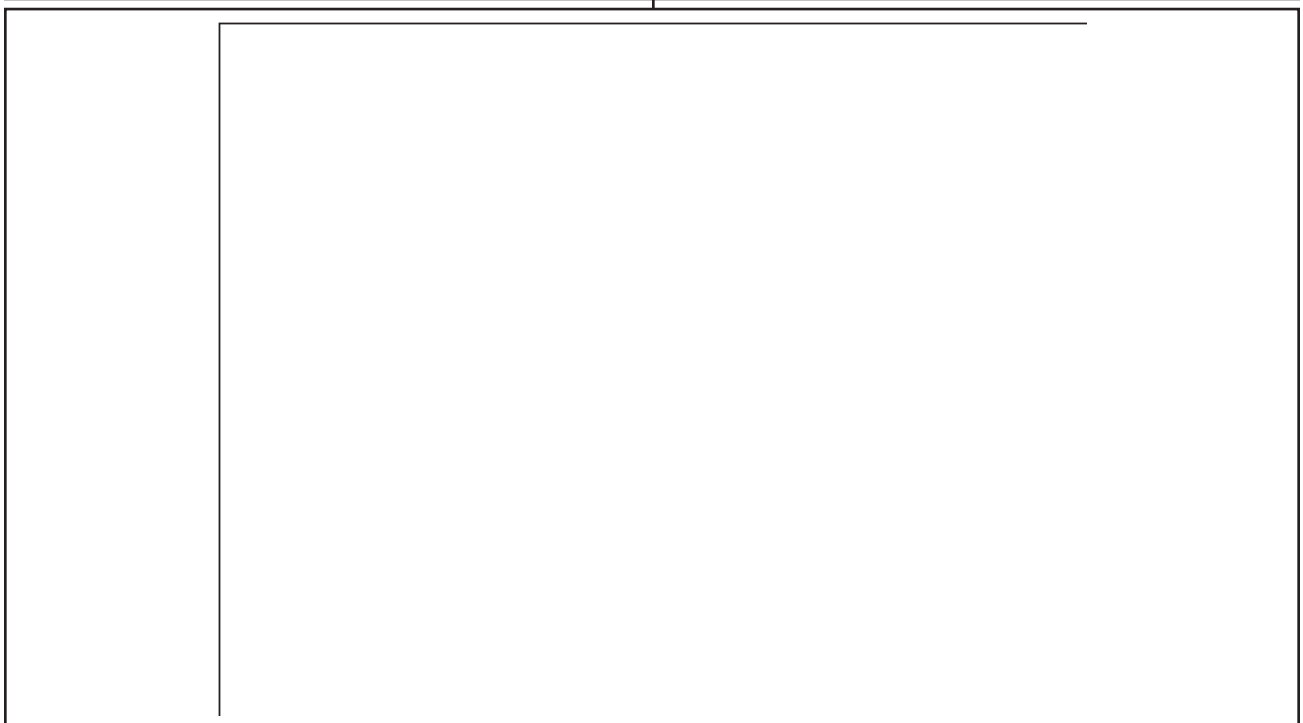

FIG. 7. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.95 POWER-FACTOR-LAGGING AT THE PREFERRED FEEDER WITH DELAY LOGIC. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) NO CROSS CURRENT

Forced-commutation technique may be used for the control logic of STS-system. This technique has been implemented in this paper and for the case under consideration. The simulation results are shown in Fig. 8. Fig. 8(a) shows the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}) and transfer time of all the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}) is 2ms. Fig. 8(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}). It shows that the transfer time of load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}) is 2ms. Hence there will be no load interruption. Fig. 8(c) shows load-side line currents (IL_a, IL_b, IL_c) having minimium transfer time i.e.$\leq$=2ms. Fig. 8(d) shows that cross current is not observed in any phase and especially in Phase-B, if forced commutation is used for outgoing thyristors of STS-Block-I

Case Study-II: 0.90 Power Factor Lagging

In this case, the STS-system has been simulated for load having power factor 0.90 lagging. Table 2 shows that cross current occurs while operating STS system at points-on-wave at 0.300, 0.301, 0.302, 0.303, 0.305, 0.306, 0.309, 0.311, 0.312, 0.313, 0.315, 0.316, 0.318, 0.319 sec. To successfully implement the delay logic technique, firing of the incoming thyristors is delayed by the time as indicated in Table 2. In some cases, these delays are beyond the permissible limits.

Simulation results are shown graphically only for one point-on-wave i.e. 0.301 sec for which maximum delay time is involved to avoid the cross current. Fig. 9 shows simulation results without any technique involved in the control logic of STS-system to avoid cross current phenomena. Fig. 9(a) shows the simulation results of the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}) and transfer time of load-side line-to-ground voltages (VL_{an}, VL_{bn}) is 2ms and is within permissible limits. While that of (VL_{cn}) is maximum and there will be a load interruption of 20ms for this phase. Fig. 9(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}) and the transfer time of load-side line-to-line voltages (VL_{bc}, VL_{ca}) is maximum

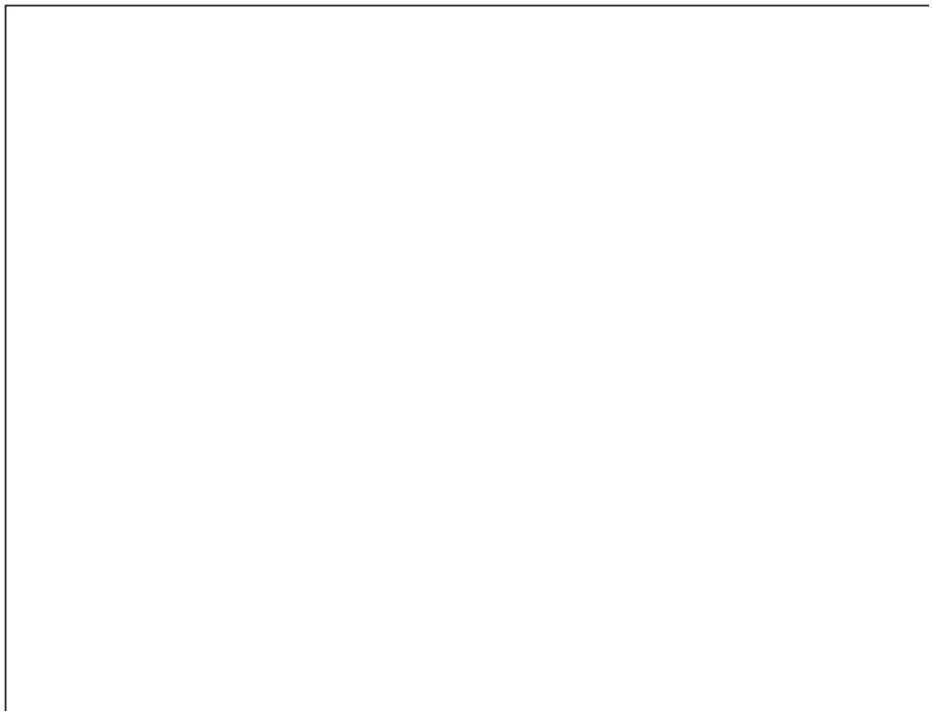

FIG. 8. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.95-POWER-FACTOR-LAGGING AT THE PREFERRED FEEDER AND FORCED COMMUTATION IS INVOLVED. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) NO CROSS CURRENT.

and load served will be interrupted for 20ms because the voltage sag is beyond permissible limit for this period. However, the transfer time of VL_{ab} is within permissible limits i.e. 2ms. Fig. 9(c) shows load-side line currents (IL_a, IL_b, IL_c). It shows that the transfer time of line-currents (IL_a, IL_b) is minimium and there is no interruption of load involved in this case. But the transfer time of line-current IL_c is maximum (i.e. 20ms) and hence load interruption will occur. Fig. 9(d) shows cross current in Phase-C and the source paralleling occurs. The transfer time is maximum because the thyristors of STS-Block-II are fired when the companion thyristors of STS-Block-I are still conducting.

Delay logic technique is implemented in the control logic of STS-system. The simulation results are shown in Fig. 10. Fig. 10(a) shows load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}). Transfer time of load-side line-to-ground voltages (VL_{an}, VL_{bn}) is 2ms and transfer time of (VL_{cn}) is 8ms. Hence load served by the Phase-C will be interrupted. Fig. 10(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}). The transfer time of load-side line-to-line voltages (VL_{ab}, VL_{bc}) is 2ms and the transfer time of load-side line-to-line voltage (VL_{ca}) is 7.7ms. Fig. 10(c) shows three-phase load-side line currents (IL_a, IL_b, IL_c). Transfer time of line-currents (IL_a, IL_b) is minimium but transfer time of line-current IL_c is maximum i.e. 6.8ms hence the load served will be interrupted. Fig. 10(d) shows no cross current in Phase-C and no source paralleling occurs.

Forced-commutation technique is implemented for the control logic of STS-system for the case under consideration. The simulation results are shown in

TABLE 2. SUMMARY OF SIMULATION RESULTS FOR 0.90 LAGGING POWER FACTOR

No.	Point-On-Wave (Sec)	Occurrence of Cross Current			Delay Time (Incoming Thyristor) (ms)
		Phase-A	Phase-B	Phase-C	
1.	0.300	Yes	x	x	3.4
2.	0.301	x	x	Yes	6.6
3.	0.302	x	x	Yes	5.8
4.	0.303	x	x	Yes	4.4
5.	0.304	x	x	x	No Delay Time
6.	0.305	x	Yes	x	6.3
7.	0.306	x	Yes	x	5.0
8.	0.307	x	x	x	No Delay Time
9.	0.308	x	x	x	No Delay Time
10.	0.309	Yes	x	x	5.7
11.	0.310	Yes	x	x	4.0
12.	0.311	x	x	Yes	6.6
13.	0.312	x	x	Yes	5.9
14.	0.313	x	x	Yes	4.5
15.	0.314	x	x	x	No Delay Time
16.	0.315	x	Yes	x	6.3
17.	0.316	x	Yes	x	5.0
18.	0.317	x	x	x	No Delay Time
19.	0.318	Yes	x	x	6.5
20.	0.319	Yes	x	x	5.6

FIG. 9. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.90 POWER-FACTOR-LOAD AT THE PREFERRED FEEDER. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) CROSS CURRENT.

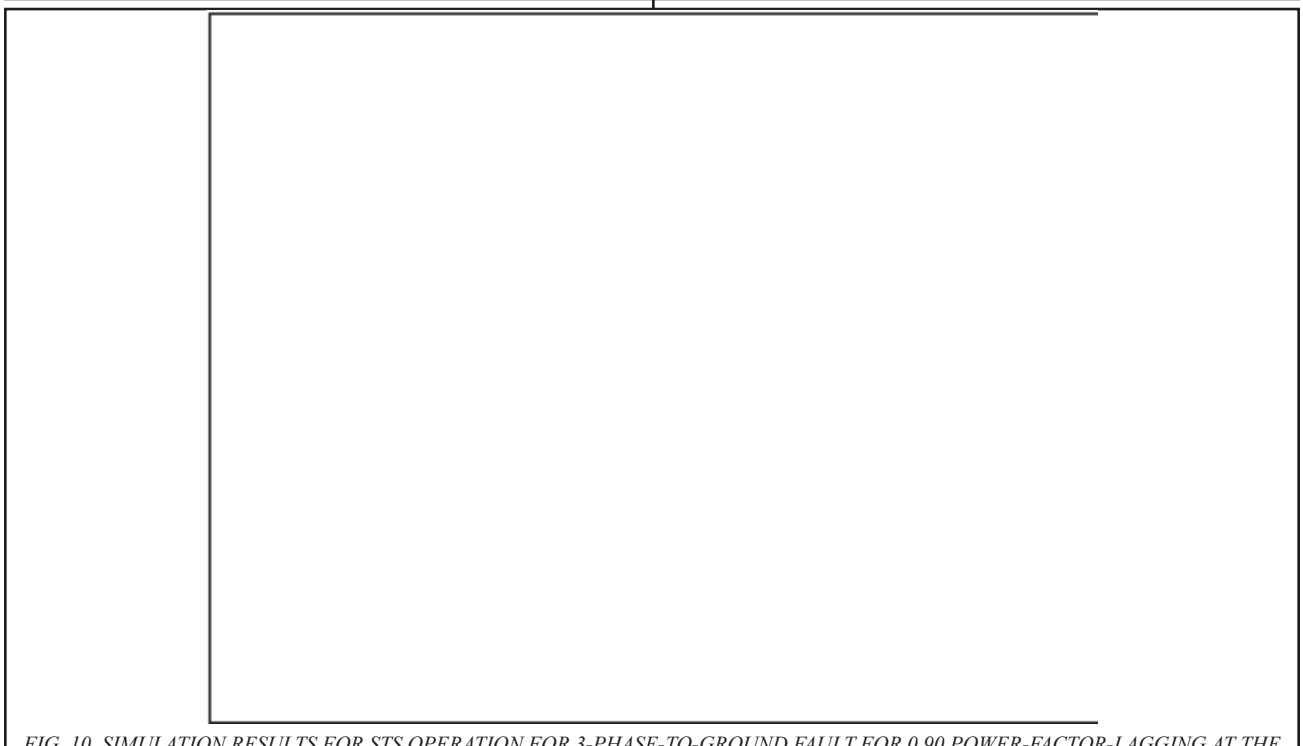

FIG. 10. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.90 POWER-FACTOR-LAGGING AT THE PREFERRED FEEDER WITH DELAY LOGIC. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) NO CROSS CURRENT

Fig. 11. The Fig. 11(a) shows the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}). By implementing forced commutation technique, the transfer time of all the load-side line-to-ground voltages (VL_{an}, VL_{bn}, VL_{cn}) becomes 2ms and is within permissible limits. Fig. 11(b) shows load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}) and transfer time of load-side line-to-line voltages (VL_{ab}, VL_{bc}, VL_{ca}) is $\leq$=2ms and is within permissible limits. Fig. 11(c) describes load-side line currents (IL_a, IL_b, IL_c) and transfer time of line-currents (IL_a, IL_b, IL_c) is $\leq$=2ms. Fig. 11(d) shows no cross current for Phase-C because of the forced commutation of outgoing thyristors of STS-Block-I.

4. CONCLUSION

In this paper, the STS-system has been effectively implemented for different load types. Different point-on-wave has been observed when preferred source is subjected to fault or disturbance. A particular one full-cycle has been studied for twenty different points on wave with a span of 18°. It is shown that forced commutation technique provides a universal solution for different disturbances as well as types of load. Delay logic technique shows limitation to transfer the varying power factor load. Forced commutation technique is fast and responsive for varying power factor loads.

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FIG. 11. SIMULATION RESULTS FOR STS OPERATION FOR 3-PHASE-TO-GROUND FAULT FOR 0.95-POWER-FACTOR-LAGGING AT THE PREFERRED FEEDER AND FORCED COMMUTATION IS INVOLVED. (A) LOAD-SIDE LINE TO GROUND VOLTAGES, (B) LOAD SIDE LINE TO LINE VOLTAGES, (C) LOAD LINE CURRENTS AND (D) NO CROSS CURRENT

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