An Intelligent Vehicular Traffic Signal Control System with State Flow Chart Design and FPGA Prototyping

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RECEIVED ON 06.06.2016 ACCEPTED ON 16.08.2016

ABSTRACT

The problem of vehicular traffic congestion is a persistent constraint in the socio-economic development of Pakistan. This paper presents design and implementation of an intelligent traffic controller based on FPGA (Field Programmable Gate Array) to provide an efficient traffic management by optimizing functioning of traffic lights which will result in minimizing traffic congestion at intersections. The existent Traffic Signal system in Pakistan is fixed-time based and offers only Open Loop method for Traffic Control. The Intelligent Traffic Controller presented here uses feedback sensors to read the Traffic density present at a four way intersection to provide an efficient alternative for better supervisory Control of Traffic flow. The traffic density based control logic has been developed in a State Flow Chart for improved visualization of State Machine based operation, and implemented as a Subsystem in Simulink and transferred into VHDL (Hardware Description Language) code using HDL Coder for reducing development time and time to market, which are essential to capitalize Embedded Systems Market. The VHDL code is synthesized with Altera QUARTUS, simulated timing waveform is obtained to verify correctness of the algorithm for different Traffic Scenarios. For implementation purpose estimations were obtained for Cyclone-III and Stratix-III.

Key Words: Traffic Signal Control, State Flow, Field Programmable Gate Array Prototyping.

1. INTRODUCTION

With rapid increase in number of vehicles the traffic congestion problems are worsening with every day, although congestion can be reduced by expansion of existing lanes and roads but at much higher cost and development time. A better alternative is to provide efficient, intelligence based traffic management at main intersections of the road network. Vehicular traffic is usually maintained by traffic signals or lights which are installed over busy intersection and junctions. Usually it is accomplished by colored lights each having distinct meaning i.e. RED=Stop, GREEN=Go etc. In Pakistan the mode of operation for these lights is usually fixed-time or PCT (Preset Cycle Time) which normally operates with pre-determined sequence and timing intervals. It is generally an unintelligent system resulting in a logically inefficient

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operation. Logical inefficiency of fixed time interval based operation becomes evident when a lane with no or less vehicular traffic is given its pre-allocated interval which may consequently increase the congestion at other lanes with more traffic. This shows that there is a need for feedback from the lanes to the controller to minimize the congestion.

The objective of this paper is to present the design and implementation of an Intelligent traffic controller which has the capability to switch the lights with adaptive intervals in accordance with the traffic density present at four lanes of the intersection and can also detect fault in sensors. The proposed application of sensors to detect the traffic density makes the controller a closed loop system, which is an improvement over the traditional open loop system. The design is implemented in two phases.

In the first phase, a control logic based on maximum traffic density is developed which combines Vehicle Actuated & Preset Cycle Time modes in state flow chart, which is tested for its operation in a Simulink model. And in the second phase, the state flow chart is converted into its equivalent VHDL code with HDL coder for FPGA prototyping. Generated VHDL code is compiled and simulated in Altera QUARTUS II to observe its correctness and performance evaluation.

1.1.1 PCT Mode

In this mode traffic light controller follows a predetermined sequence of light switching and interval length. It is basically open loop and does not take traffic density into consideration for determination of sequence or interval length. Because of open loop it's relatively easier and cheaper to design.

1.1.2 VA Mode

In this mode the already installed sensors on the lanes indicate the presence or passage of the vehicles. Based on this detection relevant lights for the particular lane are activated.

1.2 FPGA Based Prototyping

FPGA shortens development time for prototyping of newer digital designs. FPGAs usually fill the gap between ASICs (Application Specific Integrated Circuits) and microcontrollers in terms of cost, performance and speed [1]. The paper also focuses on implementation of the proposed controller design on an FPGA. FPGA require HDL for their practical implementation and unlike C or any other behavioral language it uses concurrent processing, resulting in faster operation. Verilog and VHDL are the two widely used HDLs in the world. The system model presented here is implemented with VHDL which is generated through HDL coder.

1.3 State Flow Based System Modeling

State flow is a Simulink tool which is mainly used to design an event driven system with supervisory control logic [2]. This paper also emphasis on the use of HDL coder to generate the VHDL code for the proposed control logic to reduce the overall development time. And for this purpose the state machine based model of the system is developed in State Flow, which is then transferred into its equivalent VHDL code with help of HDL coder.

This reduces the development time, achieves faster prototyping and results in high level of flexibility as any future modifications will now be done in State Flow Model of the system as compared to line by line debugging of the VHDL code of the system which consumes more time and concentration. The system is modeled as a subsystem in Simulink for functional simulation with fixed step discrete solver.

2. RELATED WORK

There are many techniques and methods which can improve the performance of traffic light system. Meisam, et. al. [3] propose a fuzzy based Intelligent algorithm that mainly operates on traffic density and other parameters to control the green light duration. The fuzzy sytem is then implemented as a State Machine in Verilog. Fuzzy systems though much efficient but require a better understanding of the fuzzy sets and how they are developed.

Jin [4] implements an FPGA state machine based inteligent controller which aims to optimize the flow of traffic. The case study has been taken as that of traffic pattern at roads of california state university, which is a localized solution.

A better improvement over a fixed time system is presented by Sabri, et. al. [5], authors present a system that operates on a fixed-time mode in the peak hours while sensors are used in the off peak hours, this also emphasize the use of sensors to improve the traffic light system even for a fixed time system. Simarpreet, et. al. [6] implement a wireless sensor network based FPGA traffic light controller. The system determines the duration of Green light by calculating the average time with the aid of counters. This system can be more complicated in terms of practical implementation. And fault in any one sensor may diminish the overall capability of the system. Another State machine based system is developed by El-Medany, et. al. [7], it presents an implementation of an FPGA based State machine controller which operates with fixed time in rush hour and uses sensors for narrow lanes in normal time. The system is built on a model having main roads and narrow lanes. Jose, et. al. [8] present a design methodolgy for FPGA based state machine controller which possess the capability to manage the flow of traffic in phase sequences, but this phase sequencing can not be generalized for other traffic intersections.

Another improvement over a fixed time system is presented by Boon, et. al. [9]. Authors propose a design which establishes improvement of a fixed time system by the time management of Peak and Off peak hour in cycles.

Liu, et. al. [10] authors emphasize the application of FPGA for the design of Dual mode traffic light controller with Master-Slave lanes, and thus it is limited for intersections having master-slave lanes. Prashant, et. al. [11] present a methodolgy with different optimized algorithms at different hours in 24 hour span with FPGA implementation.

Almost all of the cited work impose their view of better prototyping via FPGA, which is supported with their simulation results and discussion. Improvement methods of a fixed time system may seem less expensive but may require prestudy of the traffic ruotine and may be limited to specific traffic patterns. Intelligent systems based on Fuzzy and WSN (Wirless Sensor Networks) appear to be more challenging to comprehend. While state machine based control logic is more straight forward when implemented with FPGA.

3. METHODOLOGY

3.1 Four Way Intersections Model

The model presented in Fig. 1 is a generic representation of a four way intersection. It is assumed that each lane (i.e. North, South, East, West) have been installed with inductive loop sensors distanced at 5 ,10 and 15M with Sensor-1, Sensor-2 and Sensor-3 respectively at each lane. In this model the VA mode has been extended to operate on algorithm based on traffic density rather than mere presence of Vehicles.

The model uses a total of 12 sensors that are installed to cover four lanes with 3 sensors per lane. The system does not take cross lane traffic into consideration. All the traffic is presumed to flow in straight directions.

3.2 Traffic Density of Based Control Logic

This paper uses the concept of traffic density based control logic derived from similar approach used by Shwetank, et. al. [12], which demonstrates that by using multiple sensors, the controller can be prioritized to serve the lane with maximum traffic density which is given by status of sensors thereby resulting in a dynamic system.

The Fig. 2 shows the Flow Chart depicting the control logic applied in State Flow to operate as a state machine. In case of no fault the controller serves lane/s with maximum density according to sensor data as given in Table 1 Note that the Timing units 5, 10 and 15 are arbitrary and non-standard and are mainly proposed for the purpose of simulation. The objective of control logic is to maintain a correspondence between traffic density levels and Green Light's ON time duration.

3.3 Fault Detection Condition

The control logic accounts for the fault that can be logically detected. There are total 12 conditions (Table 2) for fault detection that override the normal VA based operation. When a higher numbered sensor is active and lower inactive it will be handled as a fault condition and controller will switch to PCT mode.

3.4 FPGA Based State Machine

State Machine designed in state flow chart shown in Fig. 2 is converted into VHDL for prototyping in FPGA. Workflow advisor converts the Simulink subsystem into industry standard VHDL code.

RTL view of the sate machine is represented in Fig. 3. The inputs of the State Machine are actually the sensor inputs along with clocking and enabling inputs, its outputs are essentially the states that were modeled in state flow chart. While Fig. 4 is the overall RTL model of the traffic light controller with its enabling and clocking circuitry.

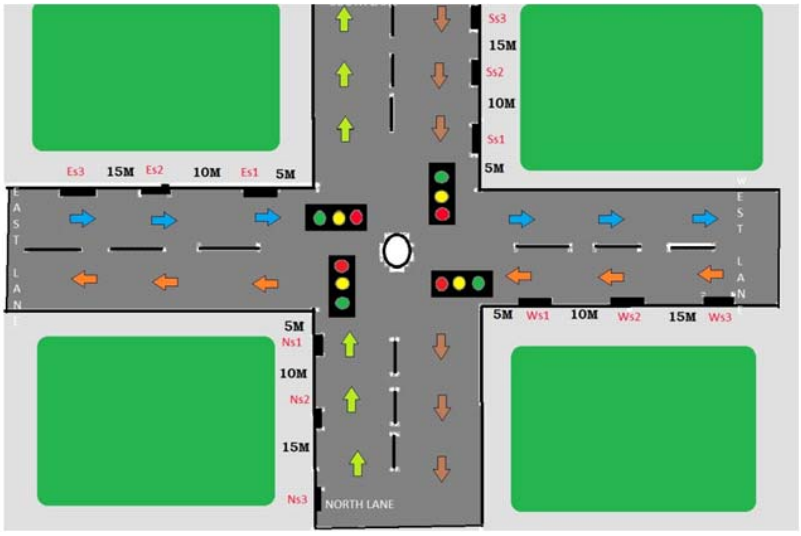

FIG. 1. FOUR WAY INTERSECTION WITH DIRECTIONS (NORTH, SOUTH EAST WEST)

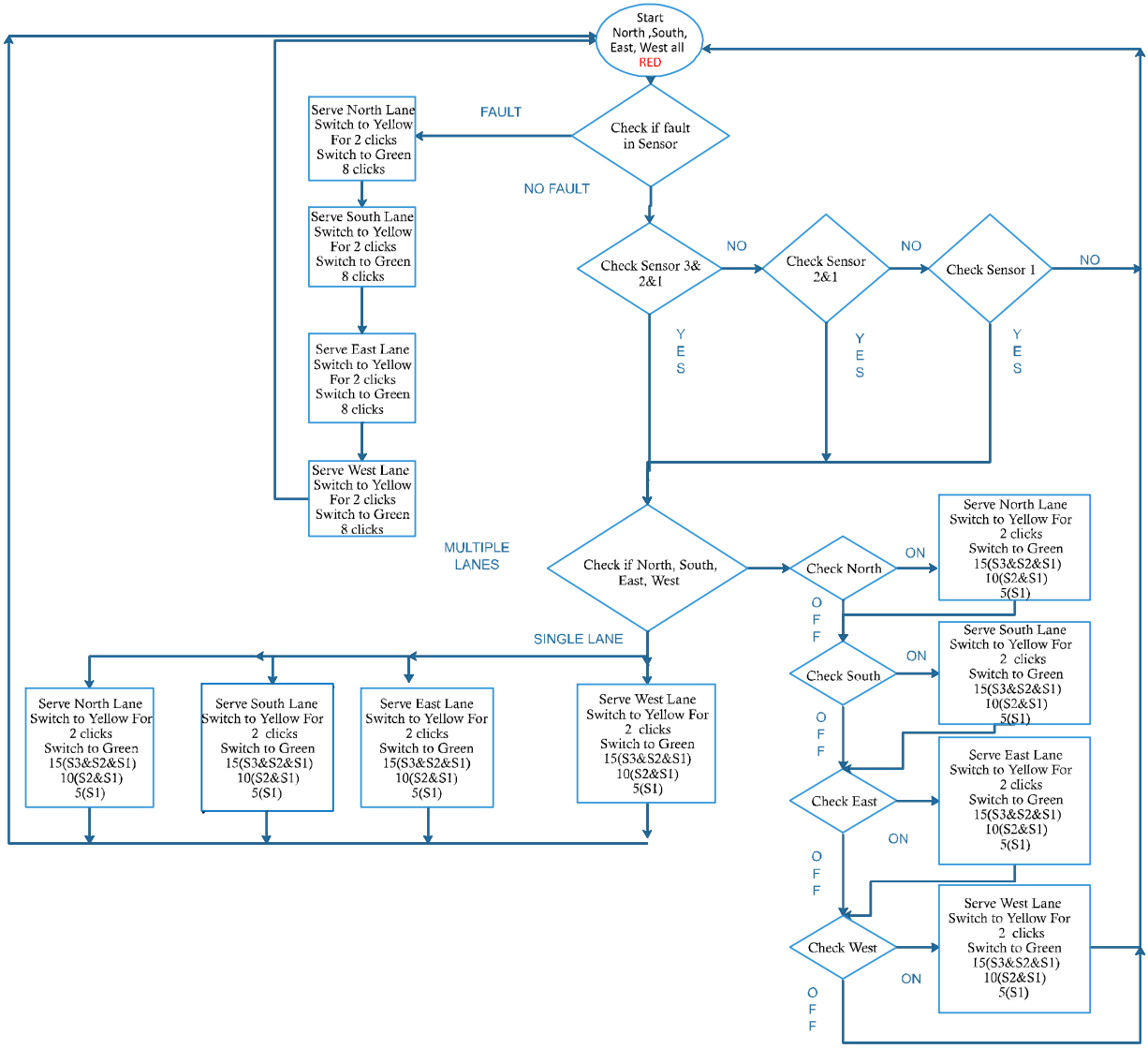

FIG. 2. FLOWCHART FOR PROPOSED CONTROL LOGIC

TABLE 1. SENSOR CONDITIONS AND DURATION OF GREEN LIGHTS

Traffic Density Level	Indication	Duration of Green Light ' ON' Time
Minimum	Only Sensor 1 is 'ON' i.e. Ns1=1, Ss1=1, Es1=1, Ws1=1	5 Clocks/Triggers
Medium	Sensor 1 &2 are 'ON' i.e. Ns1=1 && Ns2=1, | Ss1=1 && Ss2=1, Es1=1 && Es2=1, Ws1=1 && Ws2=1	10 Clocks/Triggers
Maximum	Sensor 1 ,2&3 are 'ON' i.e. Ns1=1 && Ns2=1 && Ns3=1 Ss1=1 && Ss2=1 && Ss3=1 Es1=1 && Es2=1 && Es3=1 Ws1=1 && Ws2=1 && Ws3=1	15 Clocks/Triggers

4. SIMULATION RESULTS

For the purpose of simulations Controller is subjected to different traffic situations that are manually set by sensor conditions i.e. Ns1, Ns2, Ss1 etc. The relative duration and switching instants of the Red, Green and Yellow lights are observed in response to those conditions.

TABLE 2. LIST OF SENSOR CONDITIONS READ AS FAULT

Fault Condition	Action
Ns3==1 && Ns2==0 && Ns1==0	PCT MODE
Ss3==1 && Ss2==0 && Ss1==0	
Es3==1 && Es2==0 && Es1==0	
Ws3==1 && Ws2==0 && Ws1==0	
Ns3==0 && Ns2==1 && Ns1==0	
Ss3==0 && Ss2==1 && Ss1==0	
Es3==0 && Es2==1 && Es1==0	
Ws3==0 && Ws2==1 && Ws1==0	
Ns3==1 && Ns2==1 && Ns1==0	
Ss3==1 && Ss2==1 && Ss1==0	
Es3==1 && Es2==1 && Es1==0	
Ws3==1 && Ws2==1 && Ws1==0	

Settings for Simulation

- For activation of the system 'enb' is set HIGH.
- 'resetx' is set to LOW.
- Sensor inputs for example 'Ns1', 'Ns2', 'Ns3' are set HIGH or LOW manually to depict various level traffic density for North lane. Same would be the case for other lanes.
- 'Ngreen', 'Nred' and 'Nyellow' are indications at North lane. Same would be the case for other lanes.

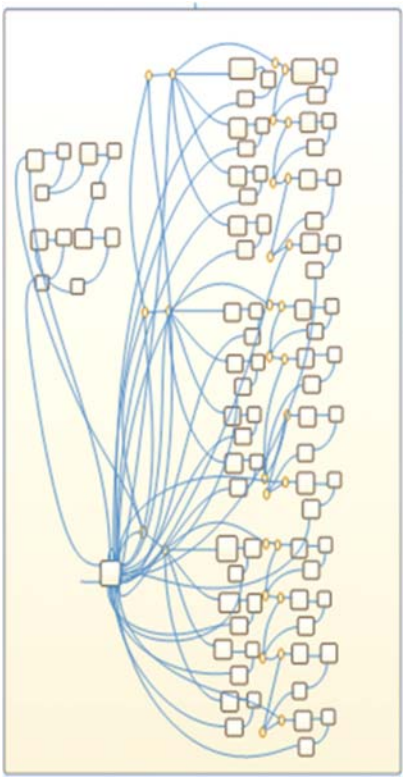

FIG. 3. STATE FLOW CHART'S BIRD EYE VIEW

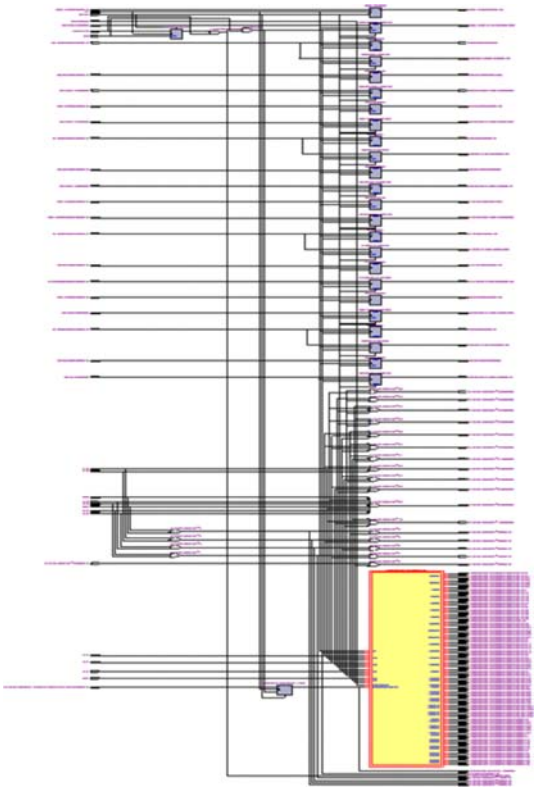

FIG. 4. BIRD EYE VIEW OF CONTROLLER

Fig. 5 shows the change in the interval of Green Light 'ON' time duration with increasing traffic density at North Lane. The controller allows more time for increased no. of vehicles to pass through the junction.

Fig. 6 shows the response of controller when the North and South lanes both attain the same level of traffic density. The system responds by opening the North lane first and then follows the South lane. This sequencing is arbitrary and non-standard, can be modified in state flow chart. The duration of Green light is in conjunction with the level of traffic density for both.

Fig.7 shows the response of the controller when different lanes are set to different levels of traffic density. The controller follows the traffic density principle by serving the lane with maximum traffic density.

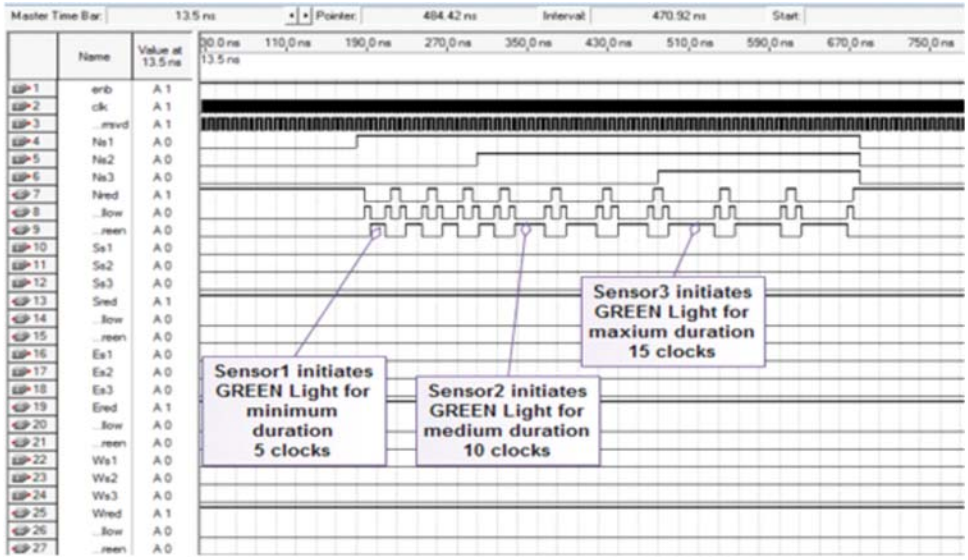

FIG. 5. NORTH HAVING GRADUAL RISE IN TRAFFIC FLOW

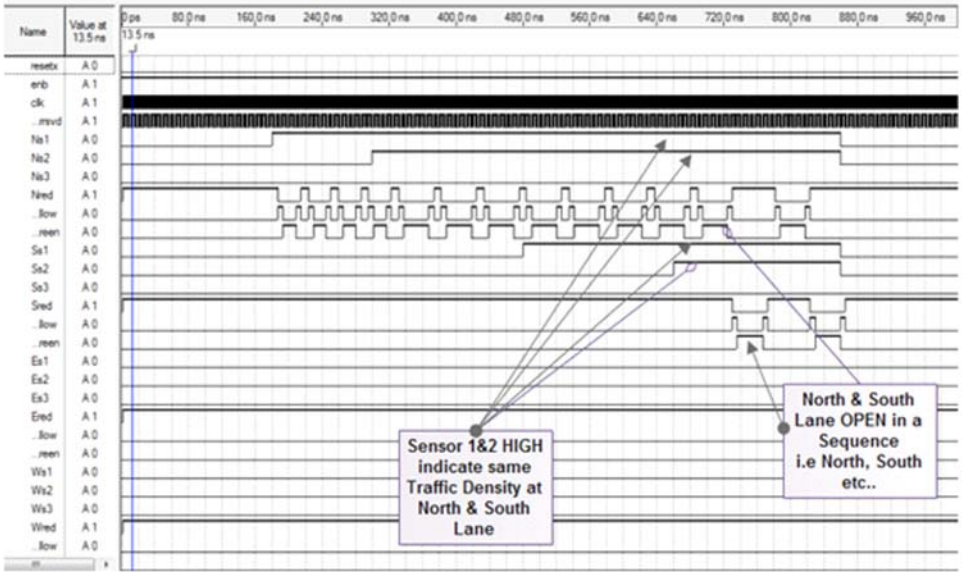

FIG. 6. RESPONSE TO NORTH & SOUTH WHEN BOTH ATTAIN SAME DEGREE OF TRAFFIC DENSITY

Fig. 8 shows the response of the system when subjected to fault conditions. In response to faults the system switches to PCT mode and serves in an orderly manner and ignores the traffic density present at lanes.

5. AREA, PERFORMANCE AND POWER

Compilation results along with Power analyzer and Time Quest analyzer reports are generated for the controller design when implemented with Stratix-III and Cyclone-III. Comparison is provided between these two FPGA devices in Tables 3-4, in terms of Area utilization, Performance in terms of Speed and Power consumption.

TABLE 3 AREA AND SPEED THROUGH COMPILATION RESULTS AND TIME QUEST ANALYZER

Area/Performance	Cyclone-III	Stratix-III
Logic Utilization	11%	1%
Registers	2%	<1%
Total I/Os	15%	9%
FMAX (MHz)	117.04	219.93

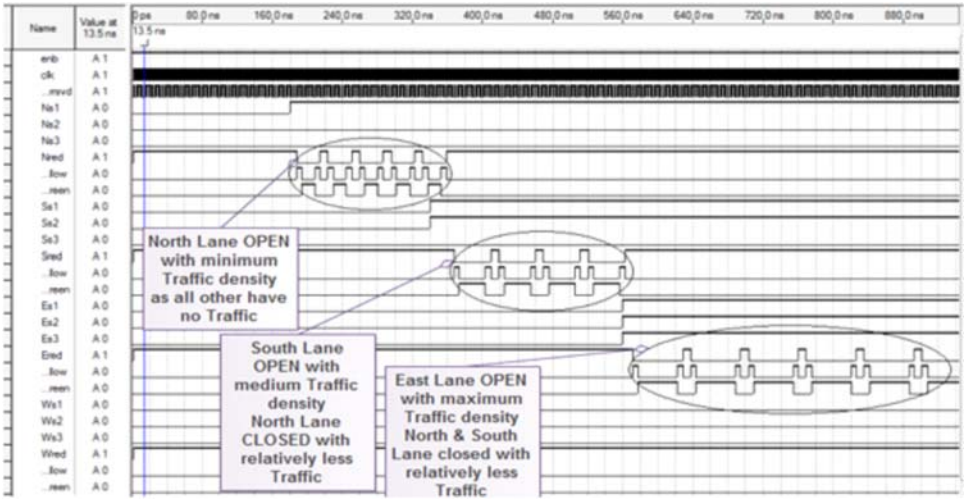

FIG. 7. RESPONSE TO DIFFERENT TRAFFIC DENSITY LEVELS

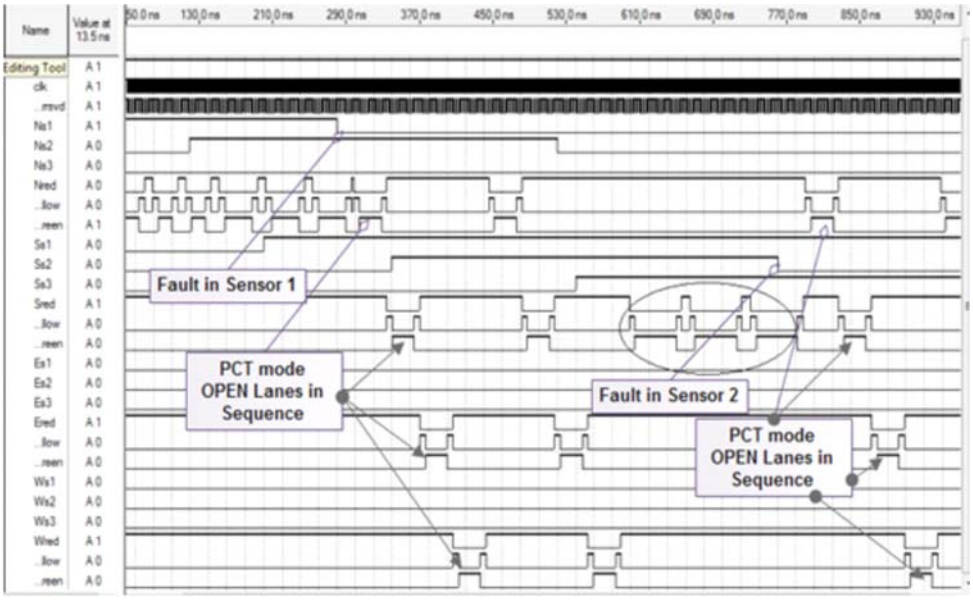

FIG. 8. SYTEM RESPONSE OVER DIFFERENT FAULT CONDITIONS

TABLE 4 POWER ANALYSIS OBTAINED BY POWER ANALYZER

Power	Cyclone-III	Stratix-III
Total Thermal Power Dissipation (mW)	105.96	485.36
Core Dynamic Thermal Power Dissipation (mW)	38.95	45.53
Core Static Thermal Power Dissipation (mW)	46.23	399.72
I/O Thermal Power Dissipation (mW)	20.78	40.29

6. CONCLUSIONS

Traffic control system presented above was successfully developed in State Flow based on Traffic Density and Fault Detection Algorithm and transferred into VHDL code using HDL coder which reduced development time. FPGA based state machine's response was observed with different conditions set by the sensors in which the controller served lane with maximum traffic density based on the proposed control logic and operated in PCT mode when subjected to fault conditions.

Compilation results, Time Quest Analyzer and Power analyzer were used to obtain Area, Performance and Power consumption reports.

In conditions where Installation costs and power consumption are major concerns Cyclone-III appears to be a better choice while Stratix-III has the capacity of expansion, and can incorporate extended network model.

This controller is an efficient alternative for the existent system of traffic light controller in Pakistan.

7. FUTURE WORK

The controller needs to be optimized with the aid of its Physical implementation along with the complete model of the system. Algorithm may be expanded to cover a complete network of traffic system, also an Alarm system may be used to signal the fault detection, and also means for fault recovery. For ASIC implementation the design may be further optimized for greater improvement in size and performance.

ACKNOWLEDGEMENTS

Authors would like to express gratitude towards Institute of Information & Communication Technologies, for their motivational drive that resulted in the completion of this research especially Prof. Dr. Mukhtiar Ali Unar, and Dr. Imtiaz Hussain Kalwar, Mehran University of Engineering & Technology, Jamshoro, and also Engr. Ayaz Ahmed Soomro, Engr. Aneela Pathan, and Engr. Shahzeb Ansari, Quaid-e-Awam College of Engineering, Science & Technology, Larkana, Pakistan, for their support and encouragement.

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